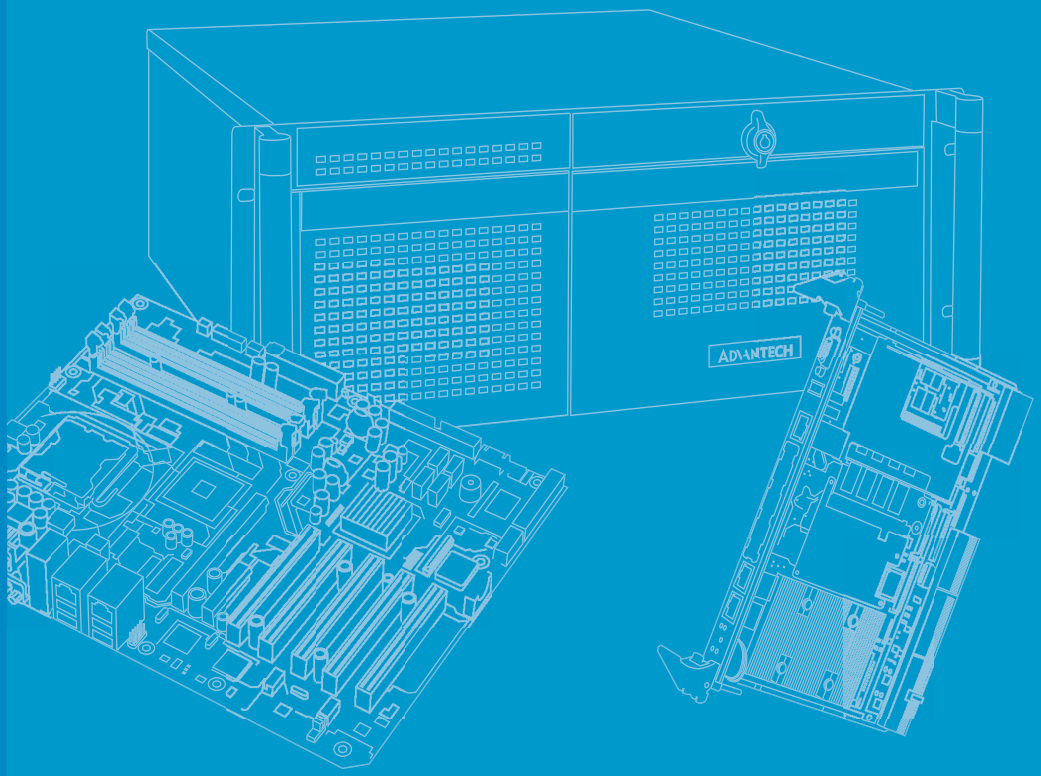

User Manual

MIC-3399

6U CompactPCI Blade SBC with 6th Gen. Intel® Core™ i3/i5/i7 Processor and Optional ECC Memory

ADVANTECH

Enabling an Intelligent Planet

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Acknowledgments

Product Warranty (2 years)

Advantech warrants the original purchaser that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products that have been repaired or altered by persons other than repair personnel authorized by Advantech, or products that have been subject to misuse, abuse, accident, or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced free of charge during the warranty period. For out-of-warranty repairs, customers will be billed according to the cost of replacement materials, service time, and freight. Please consult your dealer for more details.

If you believe your product is defective, follow the steps outlined below.

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages displayed when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain a return merchandize authorization (RMA) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a completed Repair and Replacement Order Card, and a proof of purchase date (such as a photocopy of your sales receipt) into a shippable container. Products returned without a proof of purchase date are not eligible for warranty service.
5. Write the RMA number clearly on the outside of the package and ship the package prepaid to your dealer.

Part No. 2002339900 Edition 1

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Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables.

FCC Class A

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference. In this event, users are required to correct the interference at their own expense.

FM

This equipment has passed the FM certification. According to the National Fire Protection Association, work sites are categorized into different classes, divisions, and groups based on hazard considerations. This equipment is compliant with the specifications for Class I, Division 2, Groups A, B, C, and D indoor hazards.

Technical Support and Assistance

1. Visit the Advantech website at http://support.advantech.com to obtain the latest product information.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before calling:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Warnings, Cautions, and Notes

Warning! *Warnings indicate conditions that if not observed can cause personal injury!*

Caution! *Cautions are included to help prevent hardware damage and data losses. For example,*

"Batteries are at risk of exploding if incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type as recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions."

Note! *Notes provide additional optional information.*

Document Feedback

To assist us with improving this manual, we welcome all comments and constructive criticism. Please send all such feedback in writing to support@advantech.com.

Packing List

Before system installation, check that the items listed below are included and in good condition.

- 1 x MIC-3399 all-in-one single-board computer (CPU heatsink and PCH heat-sink included)
- 1 x Daughter board for SATA HDD (assembled)
- 1 x HDD tray and screw package
- 1 x Solder-side cover (assembled)
- 1 x RJ45-to-DB9 cable
- 1 x Warranty certificate

If any of the above items are missing or damaged, contact your distributor or sales representative immediately.

Safety Instructions

1. Read these safety instructions carefully.
2. Retain this user manual for future reference.
3. Disconnect the equipment from all power outlets before cleaning. Use only a damp cloth for cleaning. Do not use liquid or spray detergents.
4. For pluggable equipment, the power outlet socket must be located near the equipment and easily accessible.
5. Protect the equipment from humidity.
6. Place the equipment on a reliable surface during installation. Dropping or letting the equipment fall may cause damage.
7. The openings on the enclosure are for air convection. Protect the equipment from overheating. Do not cover the openings.
8. Ensure that the voltage of the power source is correct before connecting the equipment to a power outlet.
9. Position the power cord away from high-traffic areas. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage from transient overvoltage.
12. Never pour liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If any of the following occurs, have the equipment checked by service personnel:
    - The power cord or plug is damaged.
    - Liquid has penetrated the equipment.
    - The equipment has been exposed to moisture.
    - The equipment is malfunctioning, or does not operate according to the user manual.
    - The equipment has been dropped and damaged.
    - The equipment shows obvious signs of breakage.
15. Do not leave the equipment in an environment with a storage temperature of below -20 °C (-4 °F) or above 60 °C (140 °F) as this may damage the components. The equipment should be kept in a controlled environment.
16. Batteries are at risk of exploding if incorrectly installed. Replace only with the same or equivalent type as recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.
17. In accordance with the IEC 704-1:1982 specifications, the sound pressure level at the operator's position does not exceed 70 dB (A).

DISCLAIMER: These instructions are provided according to IEC 704-1 standards. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Safety Precautions - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage:

- To avoid electrical shock, always disconnect the power from the PC chassis before manual handling. Do not touch any components on the CPU card or other cards while the PC is powered on.
- Disconnect the power before making any configuration changes. A sudden rush of power after connecting a jumper or installing a card may damage sensitive electronic components.

We Appreciate Your Input

Please let us know of any aspect of the product could use improvement or correction. We appreciate your valuable input in helping to make our products better.

Glossary

ACPI	Advanced configuration and power interface
API	Application programming interface
BIOS	Basic input/output system
BMC	Baseboard management controller
CLI	Command line interface
CPU	Central processing unit
DDR4	Double data rate 4
DIMM	Dual in-line memory module
DIP	Dual in-line package
ECC	Error checking and correction
FCBGA	Flip chip BGA
Flash	Flash memory
FPGA	Field-programmable gate array
FRU	Field replaceable unit
GbE	Gigabit Ethernet
GPIO	General purpose input/output
HDD	Hard disk drive
HPM.1	Hardware PlatformManagement.1
HW	Hardware
I/O	Input/output
IC	Integrated circuit
I2C	Inter-integrated circuit
IPMB	Intelligent platform management bus
IPMI	Intelligent platform management interface
KCS	Keyboard controller style
LPC	Low pin count
MAC	Medium access control
NCSI	Network controller sideband interface
NVRAM	Non-volatile random access memory
PCI	Peripheral component interconnect
PCIe	Peripheral component interconnect express
RIO	Rear input/output
RMCP	Remote management communication protocol
RS-232	Recommended standard 232
RTC	Real-time clock
RTM	Rear transition module
SATA	Serial advanced technology attachment
SDR	Sensor data record
SEL	System event log
SPD	Serial presence detect
SPI	Serial peripheral interface
SW	Software
UART	Universal asynchronus receiver transmitter
USB	Universal serial bus

Contents

Chapter 1

Hardware Configuration

This chapter describes how to configure the MIC-3399 hardware.

1.1 Introduction

Advantech's MIC-3399 series are 6U CompactPCI blade single-board computers (SBCs) with a 6th gen. Intel® Core™ i3/i5/i7/ Xeon®E3 processor and Intel® CM236 chipset. The processor uses Intel® 14 nm process technology, with a clock speed of up to 2.8 GHz and 8 MB smart cache, and supports dual-channel memory (ECC optional) of up to 32 GB DDR4 at 2133 MHz, with 16 GB onboard and one 16 GB SODIMM.

The front panel features up to six SATA in various 2.5"SATA/M.2/NAND flash form factors, five Gigabit Ethernet (including two PICMG 2.16 GbE), eleven USB, three COM, and one PS/2 interfaces that can be reserved for RTM J3/J4/J5. One PCIe x8 interface is reserved for J3 using a high-speed UHM connector with certain configurations.

Designed for harsh environments, MIC-3399 can be installed via a standard CompactPCI system slot and is ideal for datacom, telecom, military, medical, defense, and other vertical segment applications. Compliant with PICMG 2.1/2.16/2.9/2.0 Rev 3.0 specifications, MIC-3399 supports 64-bit PCI bus extensions (66/33 MHz) for up to six CompactPCI slots at +3.3 V or +5 V VIO.

1.2 Specifications

1.2.1 CompactPCI Bridge

MIC-3399 uses a Pericom PI7C9X130 universal bridge as a gateway to intelligent subsystems. When configured as a system controller, the bridge acts as a standard transparent PCIe-to-PCI/PCI-X bridge. As a peripheral controller, the local MIC-3399 processor can be used to configure and control the onboard local subsystem independently from the CompactPCI bus host processor. When MIC-3399 is in drone mode, the Pericom PI7C9X130 bridge is electrically isolated from the CompactPCI bus, receives power from the backplane, and supports the rear I/O only. The Pericom PI7C9X130 PCI bridge offers the following features:

- PCI interface
  - Full compliance with the PCI Local Bus Specification, Revision 3.0
  - Supports 3.3V PCI signaling with 5V I/O tolerance
- Supports transparent mode operations
- Supports forward bridging
- 64-bit, 66 MHz asynchronous operation
- Provides two-level arbitration support for 7 PCI bus masters
- 16-bit address decode for VGA
- Can be installed via a CompactPCI slot

For additional details, refer to the Pericom PI7C9X130 datasheet.

1.2.2 Processor

MIC-3399 supports a 6th gen. Intel® Core™ i3/i5/i7/Xeon® E3 processor with clock frequencies of up to 2.8 GHz and a Direct Media Interface (DMI) of up to 8 GT/s. Contact your local distributor or sales representative for more informations regarding processor configurations.

Table 1.1: Processor Type

Intel Model Number	CPU Architecture	# Cores	# Threads	Freq.	Cache	DMI	CPU TDP	Package	Required Airflow
i3-6100E	Sky-lake (14 nm)	2	4	2.7 GHz	3 MB	8 GT/s	35 W	FCBGA	30 CFM
I7-6822EQ	Sky-lake (14 nm)	4	8	2.0 GHz	8 MB	8 GT/s	25 W	FCBGA	30 CFM
I7-6820EQ	Sky-lake (14 nm)	4	8	2.8 GHz	8 MB	8 GT/s	45 W	FCBGA	30 CFM

Note! *Because power consumption and thermal restrictions vary between different CompactPCI systems, double check these specifications before installing a higher speed CPU not listed in the table above.*

1.2.3 Chipset

The mobile Intel® CM236 chipset provides excellent flexibility for developers of embedded applications by offering improved graphics and increased I/O bandwidth compared to previous Intel chipsets. The Intel® CM236 chipset offers up to 8 GT/s for fast access to peripheral devices and supports high-bandwidth interfaces such as PCI Express Gen III, Serial ATA Gen III, and Hi-Speed USB 2.0 and USB 3.0.

1.2.4 Memory

MIC-3399 features up to 16 GB onboard DDR4 memory with the Intel® Core™/ Xeon® processor offering support for optional ECC memory. The system also has one 260-pin SODIMM socket that can accommodate an additional 4 GB SODIMM(up to 16 GB max.). The following table lists the SODIMM modules that have been tested with MIC-3399.

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Table 1.2: Memory Type

Brand	Size	Speed	Vendor Part Number	ECC	Pin Count	Memory Chip
Advantech	16 GB	DDR4 2600	AQD-SD4U16GE26-SE	Yes	260 pin	Samsung
	16 GB	DDR4 2600	AQD-SD4U16N26-SE	No	260 pin	Samsung
	8 GB	DDR4 2600	AQD-SD4U8GN26-SE	No	260 pin	Samsung
Kingston	4 GB	DDR4 2400	KVR24S17S6/4-SP	No	260 pin	Samsung

Note! *ECC support is optional. Please contact your local sales team if you require ECC memory.*

1.2.5 Ethernet

MIC-3399 is equipped with five high-performance PCIe-based network interface controllers that are fully compliant with IEEE802.3 10/100/1000BASE-TX Ethernet. The front panel features two GbE ports (LAN1 and LAN2) and three panel-to-RTM J3/J5 connectors. One port can be switched between front panel LAN2 and RTM J5. Furthermore, MIC-3399 supports the PICMG 2.16 Packet Switching Backplane (cPSB) architecture via the J3 connector.

- Front I/O (RJ45)
- Rear I/O (rear transition module)
- PICMG 2.16

1.2.6 Storage Interface

MIC-3399 provides up to six SATA III interfaces with RAID 0/1/5/10 support. Two SATA interfaces are routed to the onboard 2.5” SATA daughter board (only one 2.5” SATA daughter board is reserved as a default); one to a SATA M.2 connector with 2242/2280 form factor; one to optional onboard NAND flash; and two to the rear I/O module.

Advantech’s RIO-3316C rear transition board is compatible with MIC-3399 and can support SATA II devices as a default and SATA III devices with the inclusion of a UHM connector upon request. Contact your local sales representative for more details.

1.2.7 Serial ports

One RJ45 COM1 port (RS-232/422/485) is provided on the front panel with one RJ45-to-DB9 adapter cable provided as an accessory. Two COM ports are routed to the rear I/O module via the J5 connector. If you encounter problems with a serial device, check the pin assignments listed in Appendix A. The IRQ and address range for these ports are fixed. If a disabled port or parameter modification is required, refer to Chapter 2.

1.2.8 USB Port

MIC-3399 provides three USB 3.0 type-A ports on the front panel and up to six USB 2.0 and three USB 3.0 interfaces via a J3/J5-to-CompactPCI connector. The MIC-3399 USB interfaces comply with USB, R2.0 and 3.0, specifications and are fuse protected (5 V @ 1.1 A).

1.2.9 System Reset and BMC Reset Button

MIC-3399 provides a system reset button located on the front panel. The system reset button resets all payload and application-related circuitry. However, it does not reset the system management (IPMI)-related circuitry. A separate BMC reset button on the front panel is provided for BMC and related hardware control.

1.2.10 XMC IEEE1386.1 Compliant

Additional I/O or co-processing functionality is supported with the inclusion of add-on XMC modules. MIC-3399 supports one single-width XMC that is fully compliant with VITA 42.0-2005 and 42.3-2006. XMC supports PCIe x8 Gen3 at 3.3V, 5V, and 12V depending on usage.

The two-layer front panel design complies with IEEE 1101.10 standard specifications. Connectors are firmly screwed into the front panel, and a shielding gasket is attached to the panel edge. This reduces emissions and increases protection from external interference.

1.2.11 Watchdog Timer

An onboard watchdog timer provides system reset capabilities via software control. The programmable time interval ranges from 1 to 255 seconds.

1.2.12 BIOS

MIC-3399 features dual 16 MB SPI flash containing specific AMI BIOS firmware with a fail-over mechanism, satisfying industrial and embedded system requirements.

1.2.13 I/O Connectivity

The MIC-3399 front panel I/O includes two RJ45 Gigabit Ethernet, one RJ45 COM, three USB 3.0, one VGA, and one XMC knockout. Rear I/O connectivity is available via CompactPCI connectors as listed below.

Different J3 connector types can be configured as HM or uHM to enable different SATA/PCIe extension speeds. For user-designed RTM boards, refer to the J3/J4/J5 pin definition information in Appendix A.

RTM Connector	Connector Type	Reserved Interface
J3	HM or uHM (optional)	■ Two SATA 3.0 ■ One PCIex8 ■ Two GbE LAN (PICMG 2.16) ■ Two USB 3.0
J4	HM	■ One LVDS ■ One DVI ■ One Audio/Mic
J5	HM	■ Two GbE (one port is switchable with front LAN2) ■ Two COM ■ Two USB 2.0 ■ One PS/2 ■ One DVI

1.2.14 Optional Rear I/O Modules

The optional rear transition module (also known as rear I/O module) designed for MIC-3399 is Advantech's RIO-3316 module. RIO-3316 offers a wide variety of I/O, including four RJ45 LAN, one RJ45 COM, two DVI, one USB 3.0, one USB 2.0, one P/S2 in the rear panel, one COM pin header, four USB 2.0 pin headers, and two SATA connectors. RIO-3316 modules are available with various I/O as shown below.

Table 1.3: RIO-3316 Configuration

RTM Model Number	Rear Panel							Onboard Pin Header/Connector				
	LAN (RJ45)	COM (RJ45)	DVI -I	DVI -D	PS/2	USB 2.0	USB 3.0	USB 2.0	SATA	COM*	Audio	Conn.
RIO-3316-C1E	4	1	1	1	1	1	1	4	2	1	1	J3, J4, J5

Note! **The onboard COM pin header is switchable with the front panel RJ45 COM port.*

1.2.15 Mechanical and Environmental Specifications

- **Operating Temperature:** 0 ~ 55 °C/-32 ~ 131 °F
- **Storage Temperature:** -40 ~ 85 °C/-40 ~ 185 °F
- **Humidity:** 95% @ 40 °C/104 °F (non-condensing)
- **Humidity (non-operating):** 95% @ 60 °C/140 °F (non-condensing)
- **Vibration:** 5~100 Hz, 2 Grms (without onboard 2.5" SATA HDD)
- **Shock:** 10 G (without onboard 2.5" SATA HDD)
- **Board Size:** 233.35 x 160 mm/9.18 x 6.29 in (6U size), 1-slot (4 TE) wide
- **Weight:** 0.8 kg (1.76 lb)

Note! *The operating temperature range of the MIC-3399 depends on the installed processor and the airflow through the chassis.*

1.2.16 Compact Mechanical Design

Forced air cooling in the chassis is recommended for MIC-3399 to optimize the system stability and reliability although a special Cu-designed heatsink is included in the unit.

1.2.17 Hardware Monitor

MIC-3399 features two types of HWM management systems. In order to monitor the processor temperature and core voltage information, NCT7904D is connected to the BMC and NCT6776D is connected to the X86 payload.

1.2.18 Super I/O

The MIC-3399 super I/O device provides the following legacy PC features:

- Serial port COM1 and COM2 are connected to J5 and can be accessed via the rear I/O module. The rear COM1 can be switched with the front panel COM via multiplexer in the FPGA.
- PS2 (keyboard/mouse) is routed to J5 and can be accessed via the rear I/O module.

1.2.19 RTC and Battery

The RTC module retains the system date and time. The MIC-3399 RTC circuitry is connected to the battery source (CR2032, 3V).

1.2.20 IPMI

MIC-3399 uses the Intelligent Platform Management Interface (IPMI) to monitor the system health. An LPC1768 microcontroller provides BMC functionality to interface between the system management software and platform hardware. MIC-3399 offers fully compliant IPMI 2.0 functionality and conforms to the PICMG 2.9 R1.0 specification. The IPMI firmware is based on proven technology from Advantech. Full IPMI details are provided in Chapter 3.

1.3 Functional Block Diagram

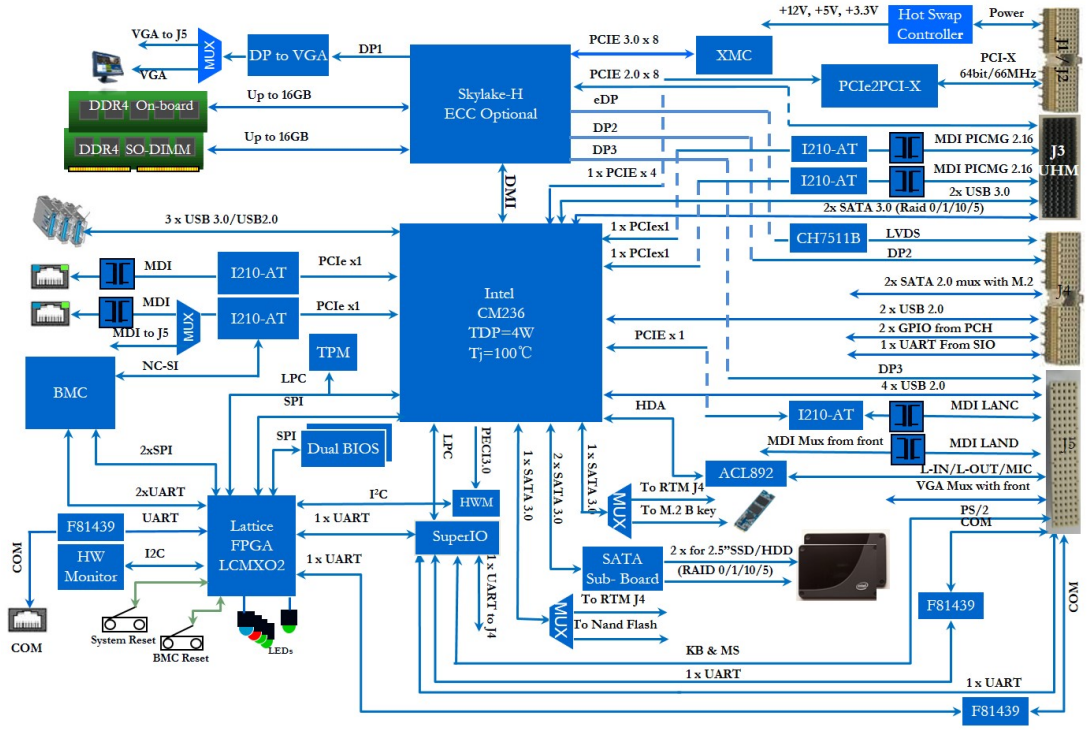


Figure 1.1 MIC-3399 Functional Block Diagram

1.4 Jumpers and Switches

The jumper and switch functions are listed in Tables 1.4 and 1.5. Read this section carefully before modifying the jumper and switch settings on the MIC-3399 board.

Table 1.4: Jumper Descriptions

Number	Function	Note
JCMOS1	Clear CMOS	
JLVDS1	Rear LVDS power voltage setting	

Table 1.5: Switch Descriptions

Number	Function	Note
SW1-1	PCI bridge clock frequency selection	
SW2-1	Switch VGA output to front panel or to rear	
SW2-2	Switch LAN output to front panel or to rear	
SW2-3	PCI bridge master/drone mode	
SW2-4	Drone mode PCI bus reset	
SW4	PEG bus configuration setting	

1.4.1 Jumper Settings

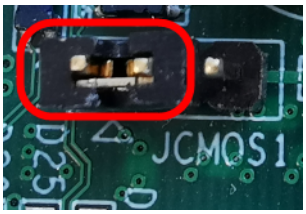
1.4.1.1 Clear CMOS (JCMOS1)

This jumper is used to erase CMOS data. Follow the procedures below to clear the CMOS.

1. Power off the system.
2. Close JCMOS1 Pins 1 and 2 for about 3 seconds.
3. Then close JCMOS1 Pins 2 and 3, as per the Normal setting.
4. Power on the system. The BIOS will be restored to the default settings.

Table 1.6: JCMOS1 Clear RTC

Status	Function	Note
Closed 1-2	Clear RTC	
Closed 2-3	Normal	[default]



JCMOS1 Closed 1-2

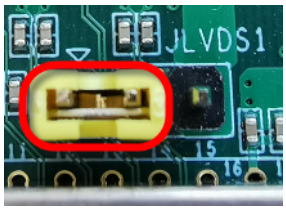
JCMOS1 Closed 2-3

1.4.1.2 Rear LVDS Setting (JLVDS1)

This jumper is used to configure the LVDS power settings.

Table 1.7: JLVDS1 Settings

Status	Function	Note
Closed 1-2	LVDS for 3.3V LVDS panel	[default]
Closed 2-3	LVDS for 5V LVDS panel	



JLVDS1 Closed 1-2

JLVDS1 Closed 2-3

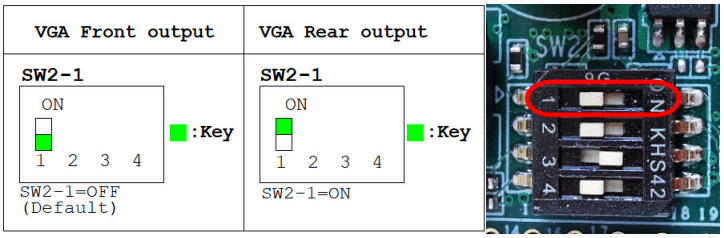
1.4.2 Switch Settings

1.4.2.1 VGA Output (SW2-1)

This switch is used to switch VGA output from the front panel to the rear I/O.

Table 1.8: SW2-1 Switch VGA Output

Status	Function	Note
Off	Front panel	[default]
On	Rear I/O	

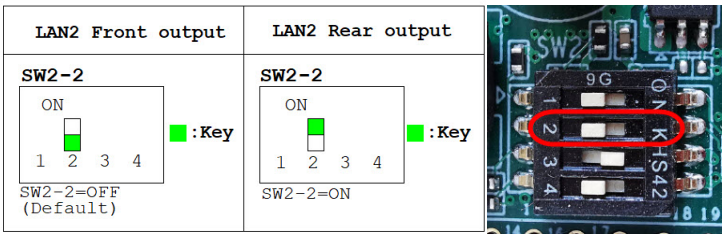


1.4.2.2 LAN2 Output (SW2-2)

This switch is used to switch LAN2 output from the front panel to the rear I/O.

Table 1.9: SW2-2 Switch LAN2 Output

Status	Function	Note
Off	Front panel	[default]
On	Rear I/O	

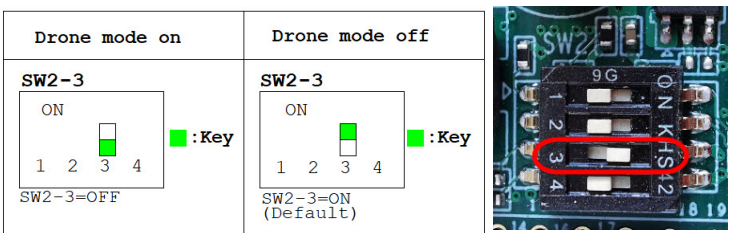


1.4.2.3 PCI Bridge Master/Drone Mode (SW2-3)

This switch is used to switch the PCI bridge between Master and Drone modes.

Table 1.10: SW2-3 Switch PCI Bridge Mode

Status	Function	Note
Off	Drone mode	
On	Master mode	[default]

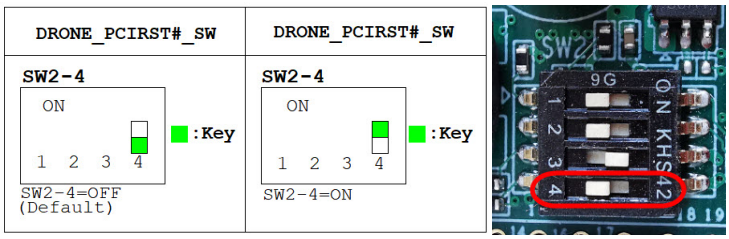


1.4.2.4 Drone Mode Settings (SW2-4)

This switch is used to switch to Drone mode with or without J1_RST.

Table 1.11: SW2-4 Drone Mode Settings

Status	Function	Note
Off	Drone mode w/o J1_RST	[default]
On	Drone Mode w/ J1_RST	

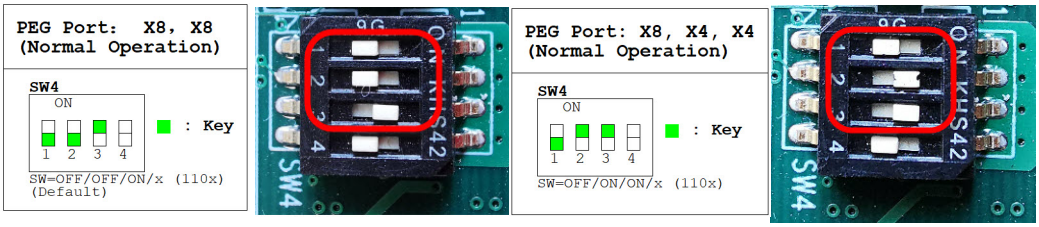


1.4.2.5 PCIE Bus Settings (SW4)

This switch is used to configure the PCIe mode settings.

Table 1.12: SW4 PCIE Mode Settings

Status	Function	Note
Off/Off/On/X	XMC:1 x PCIe x8 Rear J3: 1 x PCIe x8	[default]
Off/On/On/X	XMC:1 x PCIe x8 Rear J3: 4 x PCIe x4	



1.4.3 RIO-3316-C1E DIP Switch Settings

Table 1.13: SW3 and SW4 for Internal COM1

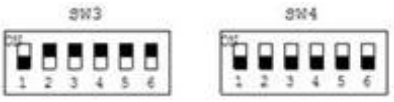
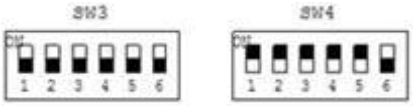
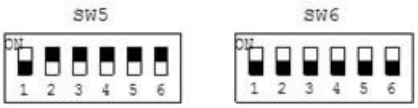
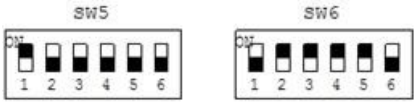
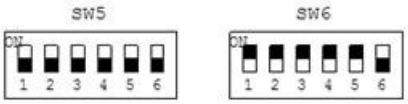
Status	Function	Note
[Default]	RS-232	
	RS-422	
	RS-485	

Table 1.14: SW5 and SW6 for COM2

Status	Function	Note
[Default]	RS-232	
	RS-422	
	RS-485	

These switches are only available for the RIO-3316-C1E model.

1.5 Connector Definitions

The function of each connector is listed Table 1.15, and the location of each connector is shown in Figs. 1.2 and 1.3.

Table 1.15: Onboard Connector Descriptions

Number	Function	Note
SATA1	SATA HDD daughter board	
M.2CN1	2242 or 2280 M.2 socket	
XMC1	XMC socket	
DIMM1	DDR4 SODIMM socket	
J1/J2	Primary CompactPCI bus	
J3/J4/J5	Rear I/O transition	

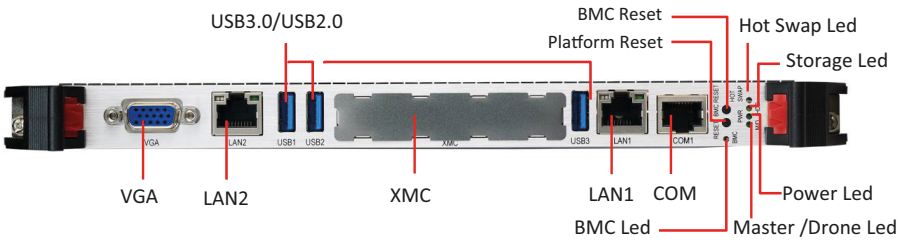


Figure 1.2 MIC-3399 Front Panel Ports, Indicators, and Buttons

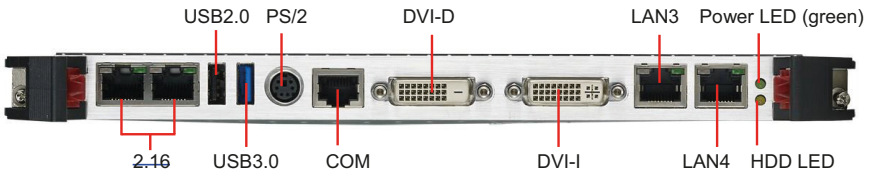


Figure 1.3 RIO-3316-C1E Front Panel Ports and Indicators

1.6 Safety Precautions

Follow the simple precautions below to protect yourself from harm and the products from damage.

- To avoid electric shock, always disconnect the power from the CompactPCI chassis before manual handling. Do not touch any components on the CPU board or other boards while the CompactPCI chassis is powered on.
- Disconnect the power before making any configuration changes. A sudden rush of power when connecting a jumper or installing a board may damage sensitive electronic components.
- Always ground yourself to remove any static charge before touching the CPU board. Be particularly careful not to touch the chip connectors.
- Modern integrated electronic devices, especially CPUs and memory chips, are extremely sensitive to static electric discharges and fields. Keep the board in the antistatic packaging when not installed in the chassis, and place the board on a static dissipative mat when working with it. Moreover, wear a grounding wrist strap for continuous protection.

1.7 Hardware Installation

MIC-3399 contains electrostatic-sensitive devices. Please discharge static electricity from your clothing before touching the assembly. Do not touch components or connector pins. We recommend that you perform assembly at an antistatic workbench.

1.7.1 HDD Installation

MIC-3399 supports a 2.5” SATA hard disk drive. The SATA HDD daughter board is pre-assembled on the MIC-3399 SBC, but the SATA HDD brackets are not. The brackets and screws are provided in the accompanying accessory box. Instructions for installing the SATA HDD are provided below.

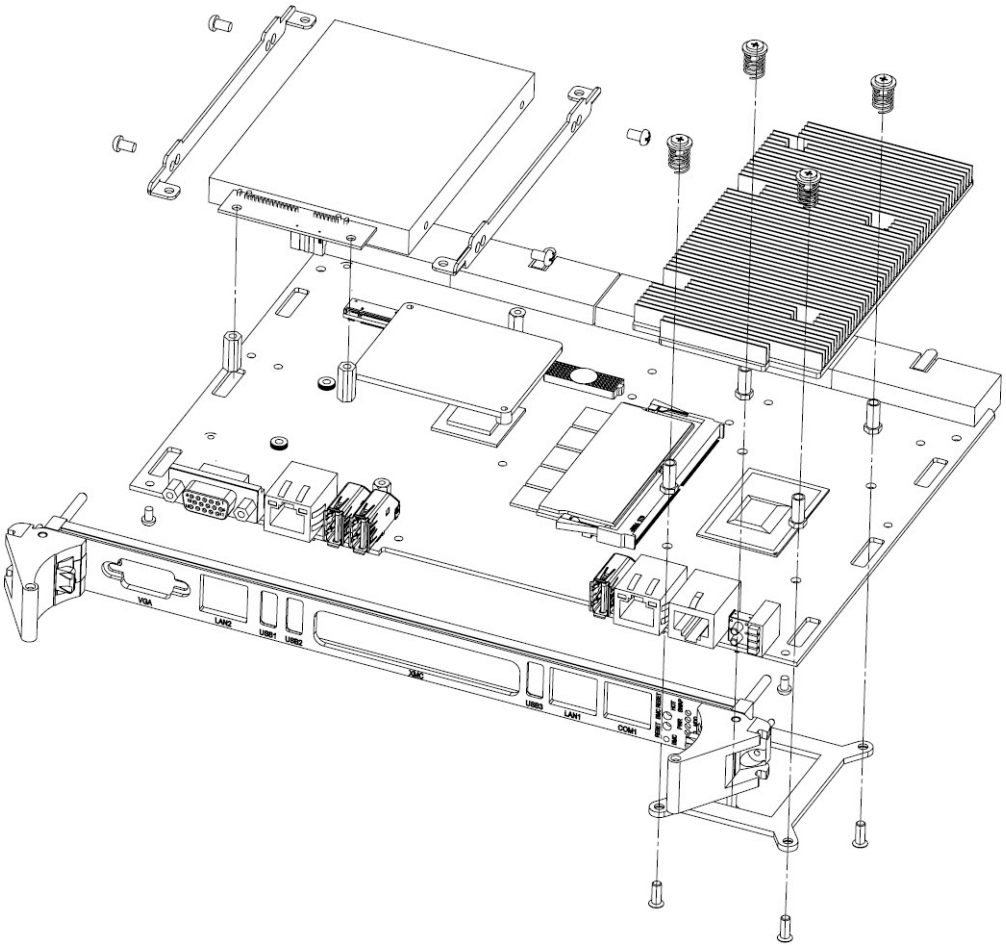


Figure 1.4 MIC-3399 Assembly with 2.5” HDD

1. Attach the HDD brackets to the side of HDD and use 4 x M3 screws to fasten them in place.

Figure 1.5 Attach the SATA HDD to the HDD brackets

2. Install the SATA HDD attached to the brackets into the chassis. Connect the SATA HDD to the SATA connector. Fasten the HDD in place using 4 x M2.5 screws as show in Fig. 1.6.

Figure 1.6 Installing the SATA HDD into the Chassis

1.8 Battery Replacement

MIC-3399 is equipped with a 3V battery (Advantech part number: CR2032). Replacement batteries can be purchased from Advantech. Contact your local sales representative to check availability.

1.9 Software Support

MIC-3399 has been tested and verified to support Windows 7/10, Linux, and VxWorks 6.9/7.0 operating systems. Contact your local sales representative for advice regarding other operating systems.

Chapter 2

AMI BIOS Setup

This chapter describes how to configure the AMI BIOS.

2.1 Introduction

The AMI BIOS ROM features a built-in BIOS Setup program specifically adapted for MIC-3399 that allows users to modify the basic system configuration and function settings. The BIOS Setup program features a number of menus for adjusting various items. This chapter describes the basic navigation of the BIOS Setup menus and explains how to configure the BIOS settings.

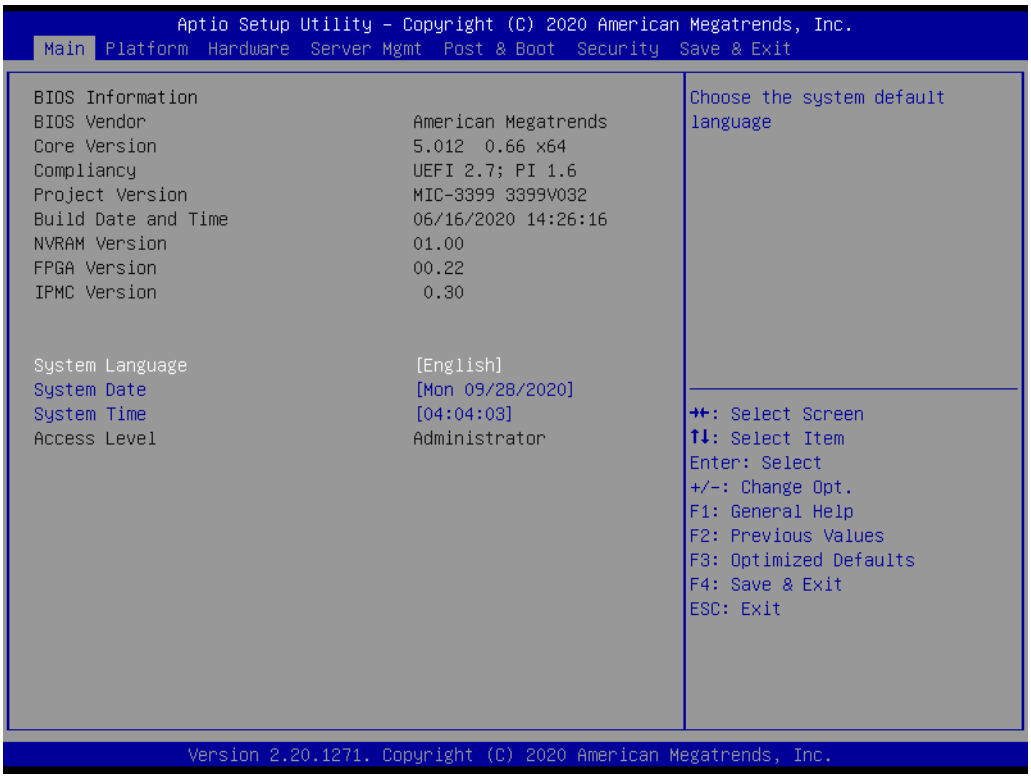


Figure 2.1 BIOS Setup Utility Main Menu

2.2 BIOS Setup Utility

The BIOS Setup Utility saves the system configuration settings in the NVRAM of the motherboard. When the system power is turned off, the battery on the board supplies the necessary power to retain the system configuration settings. However, when the CMOS battery is removed or the “clear CMOS” jumper is set, all settings will be restored to the default BIOS settings.

Control Keys	
< → > < ← >	Select Screen
< ↑ > < ↓ >	Select item
<Enter>	Select
<+/->	Change option
<F1>	General help, go to setup submenu
<F2>	Previous values
<F3>	Optimized defaults
<F4>	Save & exit
<Esc>	Exit

2.3 Entering the BIOS

When the system is powered on, press <Del> or <F2> during the BIOS power-on self test to access the BIOS Setup Utility.

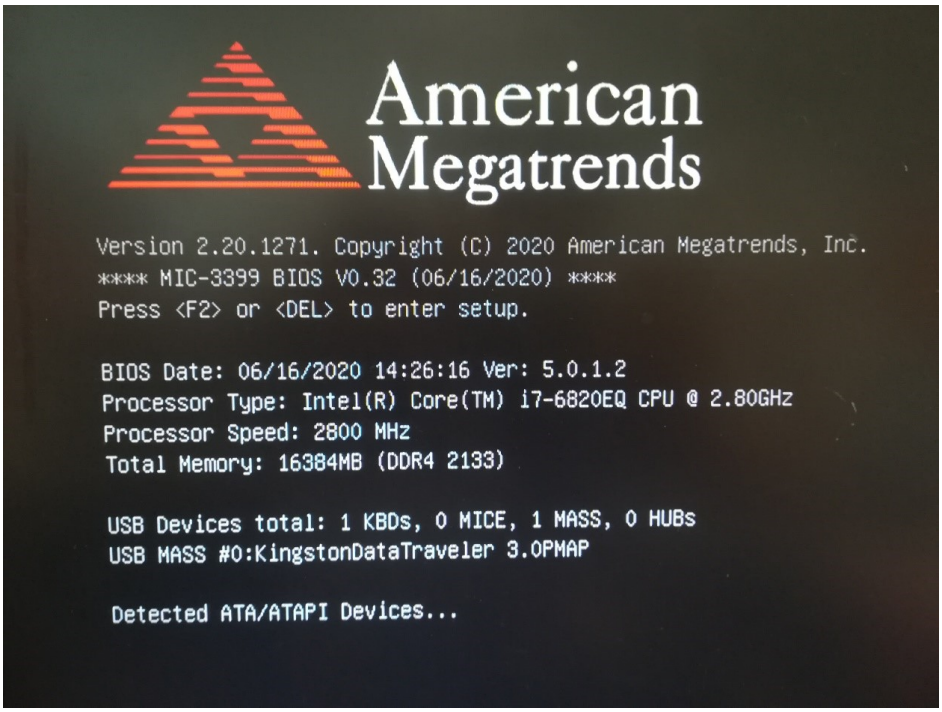


Figure 2.2 BIOS POST Screen

2.3.1 Main Screen

Upon entering the BIOS Setup utility, users are presented with the Main setup page. Users can always return to the Main setup page by selecting the Main tab. The Main BIOS Setup page is shown below.

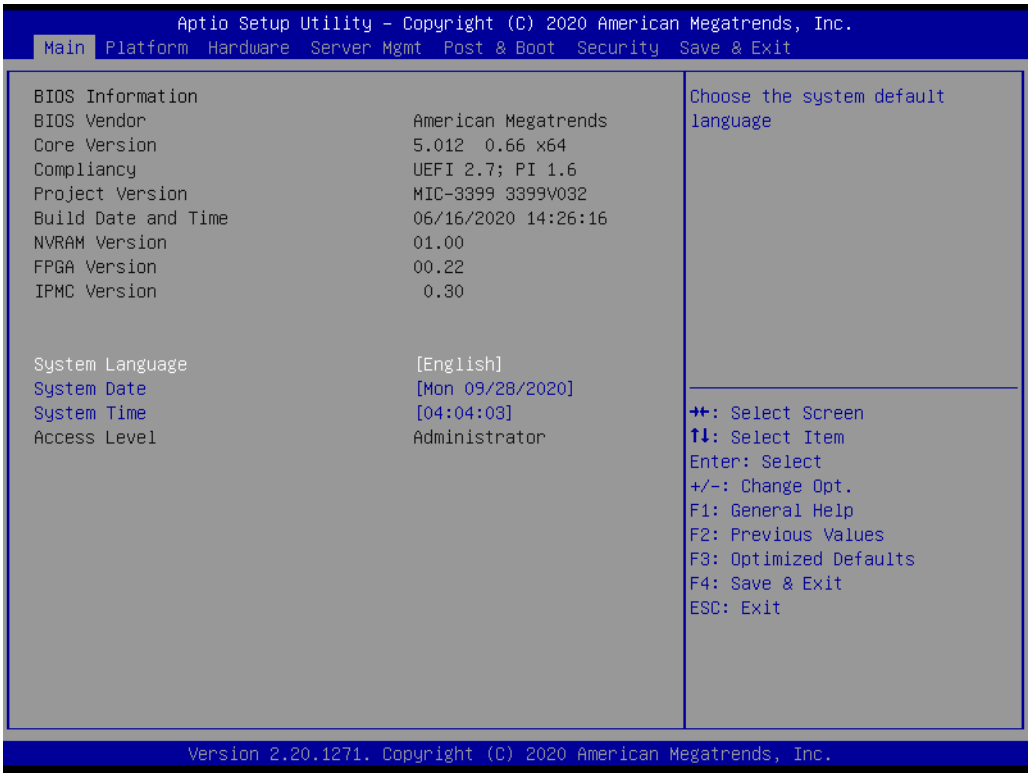


Figure 2.3 Main BIOS Setup Page

The Main BIOS setup page has two main frames. The left frame displays all the items accessible on the Main page. Items that are grayed out cannot be configured, whereas items presented in blue text can be configured. The right frame displays the key legend.

Located above the key legend is an area reserved for a text message. When an item is selected in the left frame, the item is presented in white text and often accompanied by a text message.

- **System Time/System Date**
  Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values via the keyboard. Press <Tab> or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format, and the time must be entered in HH:MM:SS format.

2.3.2 Platform Settings

Click on the Platform tab to enter the Platform setup menu. Users can click on the items in the left frame of the screen, such as Serial Console, to access the submenu for that item. Use the <↑> and <↓> keys to move between items and view the item options.

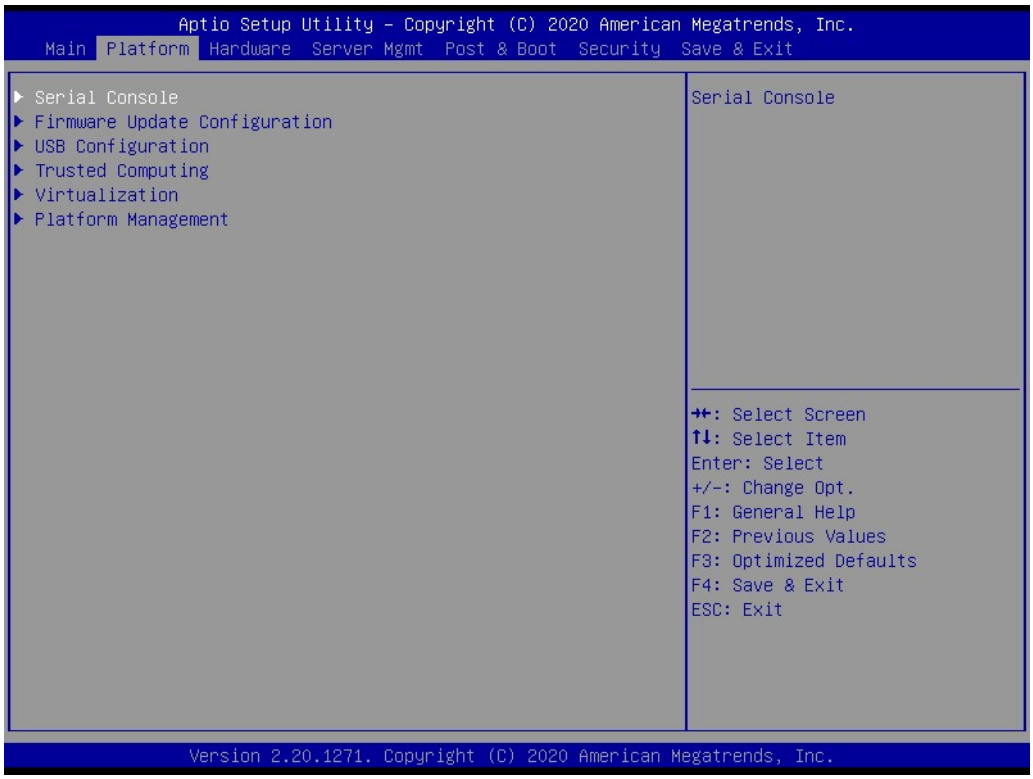


Figure 2.4 Platform BIOS Setup Page

2.3.2.1 Serial Console Setting

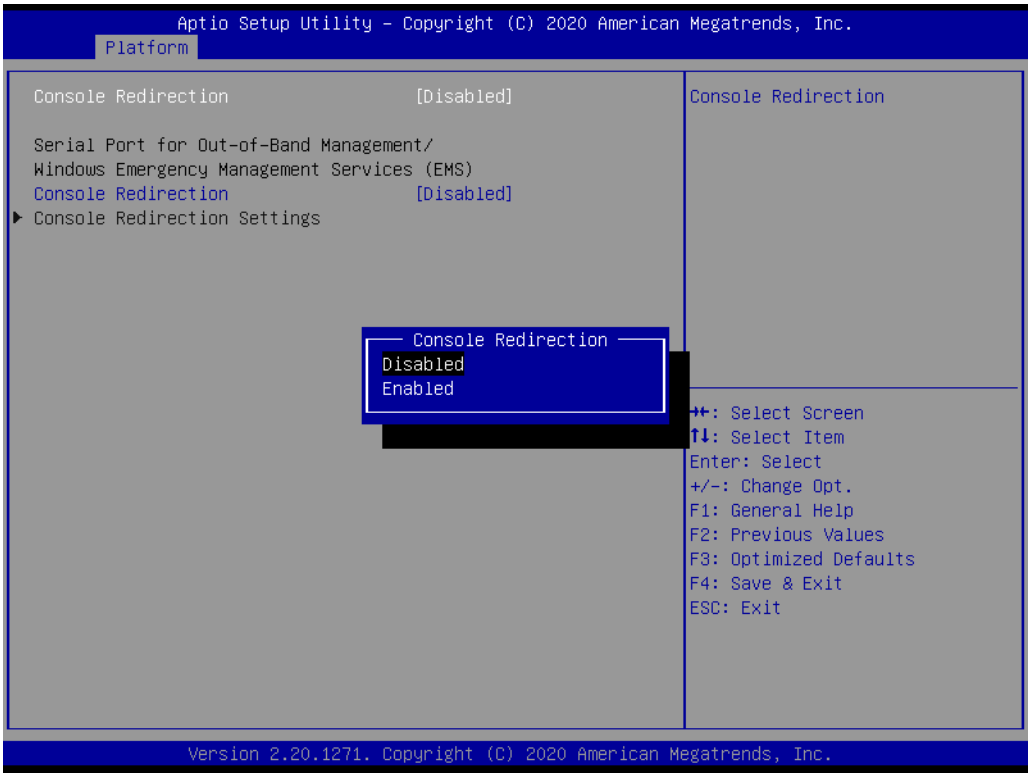


Figure 2.5 Serial Console Setting

- **Console Redirection**
  This item allows users to enable/disable console redirection or Microsoft Windows Emergency Management Services (EMS).

2.3.2.2 Firmware Update

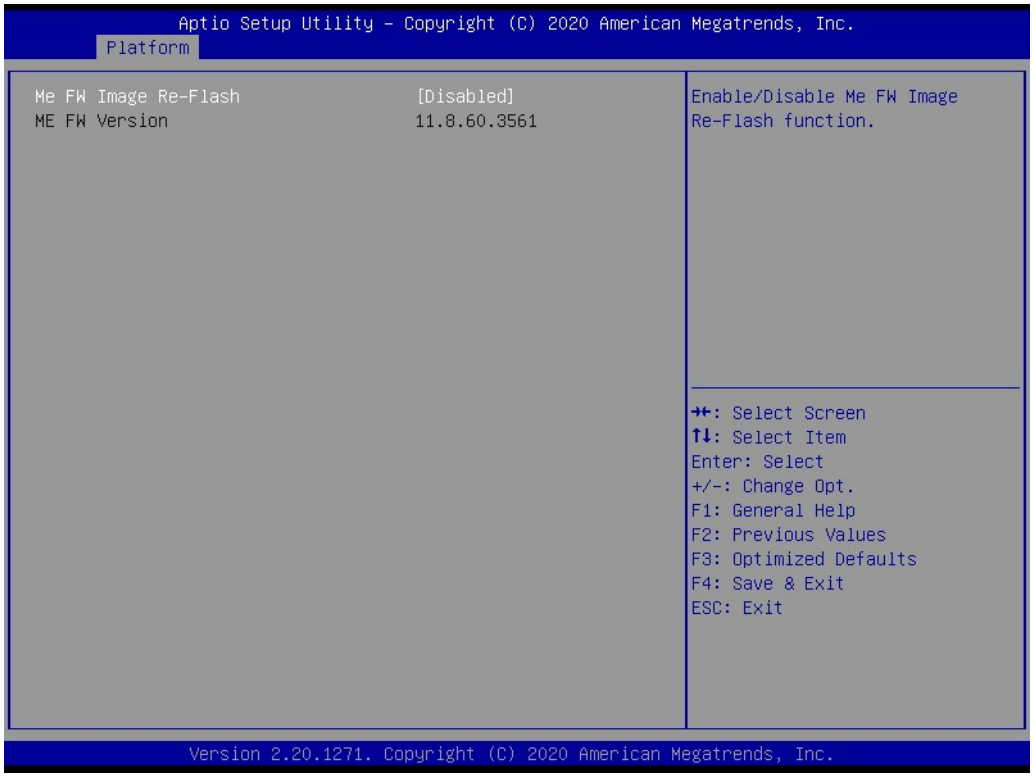


Figure 2.6 Firmware Update

- **ME FW Image Re-Flash**
  This item allows users to enable/disable the ME firmware image re-flash function.

2.3.2.3 USB Configuration

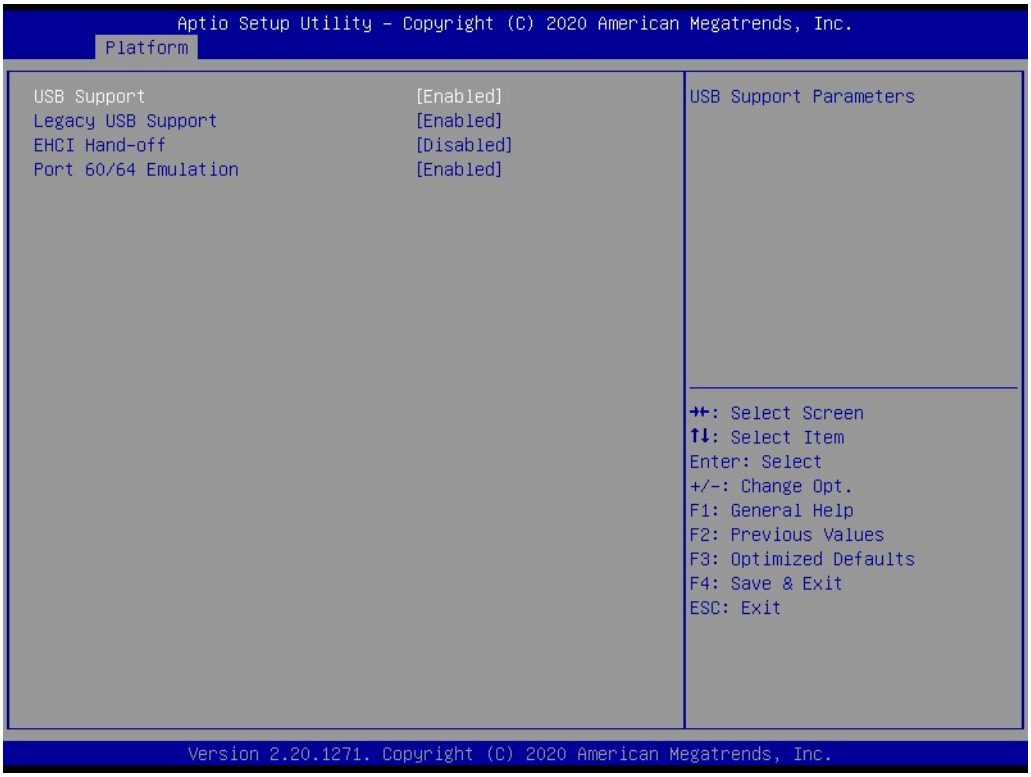


Figure 2.7 USB Configuration

- **USB Support**
  This item allows users to configure the USB support parameters.
- **Legacy USB support**
  This item allows users to enable/disable legacy USB support. The auto option disables legacy support if no USB devices are connected. The disable option will keep USB devices available only for EFI applications. The default setting is enabled.
- **EHCI Hand-Off**
  This is a workaround for operating systems without EHCI hand-off support. Any EHCI ownership changes should be conducted by the EHCI driver.
- **Port 60/64 Emulation**
  This item allows users to enable/disable support for I/O port 60h/64h emulation. This should be enabled for complete USB keyboard legacy support for non-USB aware operating systems.

2.3.2.4 Trusted Computing

Figure 2.8 Trusted Computing

- **Security Device Support**
  This item allows users to enable/disable BIOS support for security devices.
- **SHA-1 PCR Bank**
  This item allows users to enable/disable SHA-1 PCR banks.
- **SHA256 PCR Bank**
  This item allows users to enable/disable SHA256 PCR banks.
- **Pending Operation**
  This item allows users to schedule an operation for a security device.
  NOTE: The computer must reboot to change the status of a security device.
- **Platform Hierarchy**
  This item allows users to enable/disable platform hierarchy.
- **Storage Hierarchy**
  This item allows users to enable/disable storage hierarchy.
- **Endorsement Hierarchy**
  This item allows users to enable/disable endorsement hierarchy.
- **TPM2.0 UEFI Spec Version**
  This item allows users to select the TCG2 spec version to support.
  TCG_1_2: The compatible mode for Windows 8/10.
  TCG_2: The new TCG2 protocol and event format for Windows 10 or later.
- **Physical Presence Spec Version**
  This item allows users to select whether the OS supports PPI Spec Version 1.2 or 1.3. NOTE: Some HCK tests may not support Version 1.3.
- **Device Select**
  This item allows users to select the supported devices. TPM 1.2 will restrict support to TPM 1.2 devices. TPM 2.0 will restrict support to TPM 2.0 devices. The Auto option means both are supported, with the default set to TPM 2.0 devices. If not found, TPM 1.2 devices will be enumerated.

2.3.2.5 Virtualization

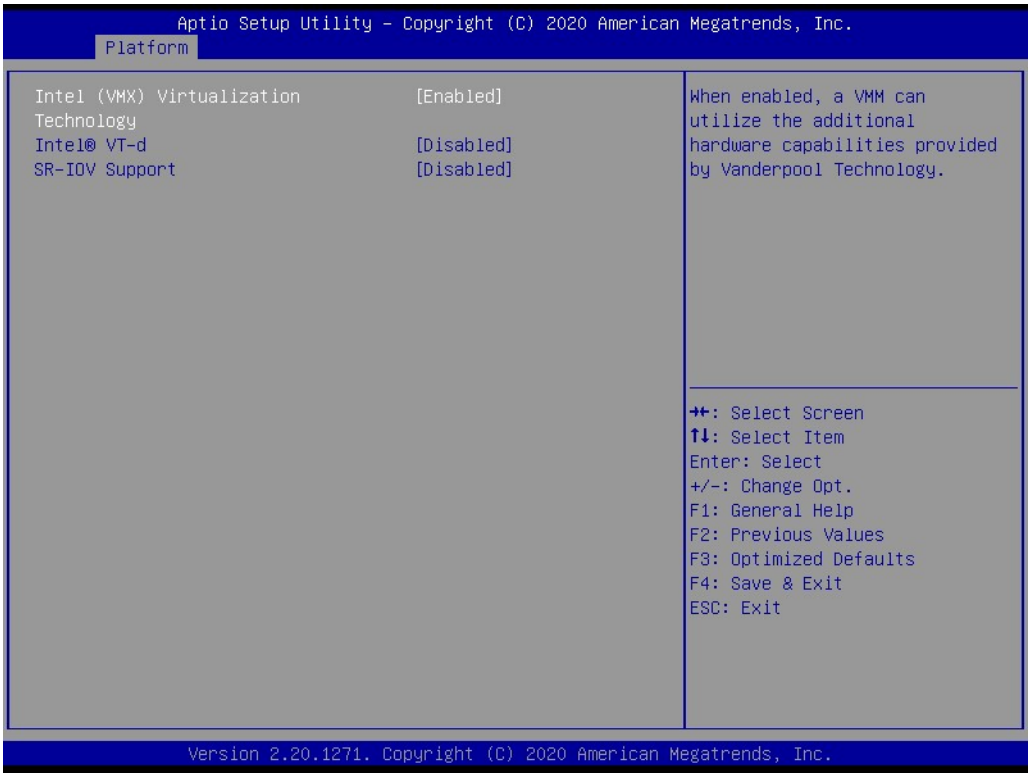


Figure 2.9 Virtualization

- **Intel(VMX) Virtualization Technology**
  This item allows users to enable/disable Intel Virtualization Technology. When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.
- **Intel®VT-d**
  This item allows users to enable/disable VT-d capability.
- **SR-IOV Support**
  This item allows users to enable/disable single root I/O virtualization support, if the system has SR-IOV-capable PCIe devices.

2.3.2.6 Platform Management

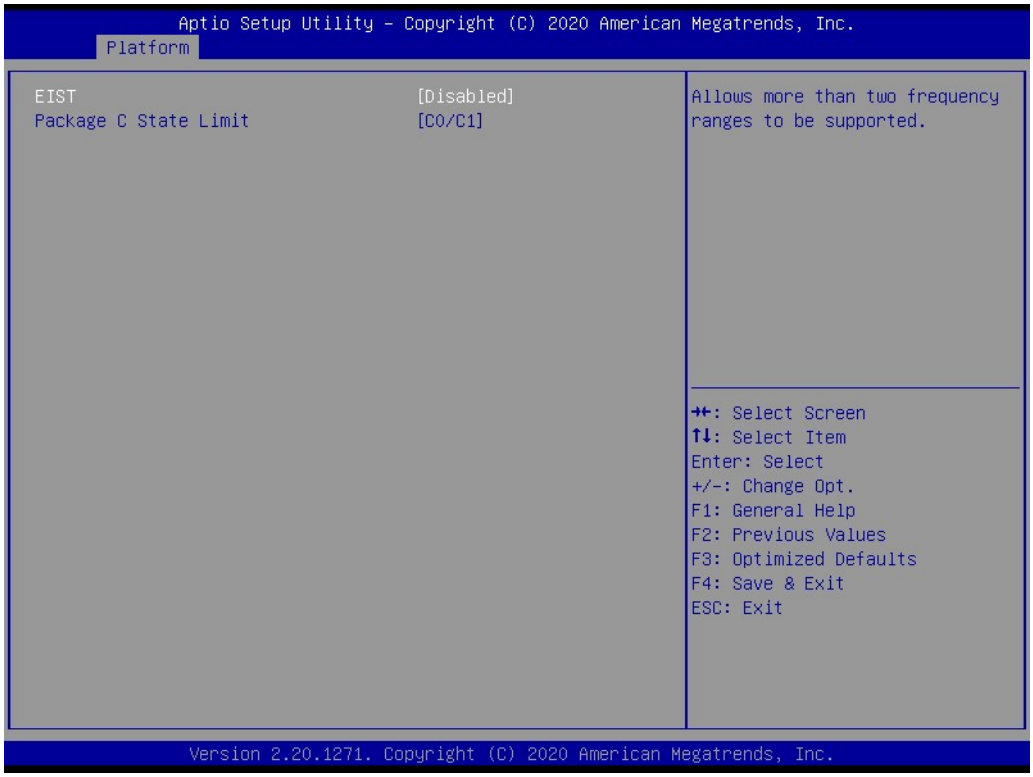


Figure 2.10 Platform Management

- **EIST**
  This item allows users to configure the system to support more than two frequency ranges.
- **Package C State Limit**
  This item allows users to configure the maximum package C state limit.
  CPU default: Retains the factory default value.
  Auto: Initiates the deepest available package C state limit.

2.3.3 Hardware Settings

Select the Hardware tab to enter the Hardware setup menu. Users can select any item in the left frame of the screen to access the submenu for that item.

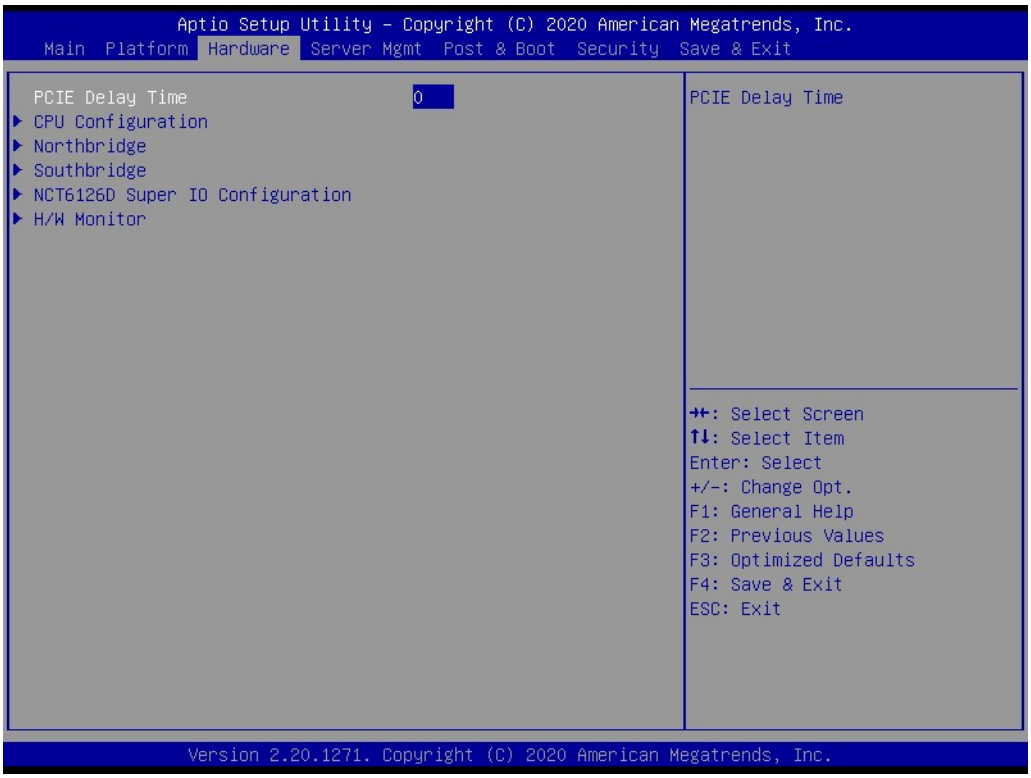


Figure 2.11 Hardware BIOS Setup Page

2.3.3.1 CPU Configuration

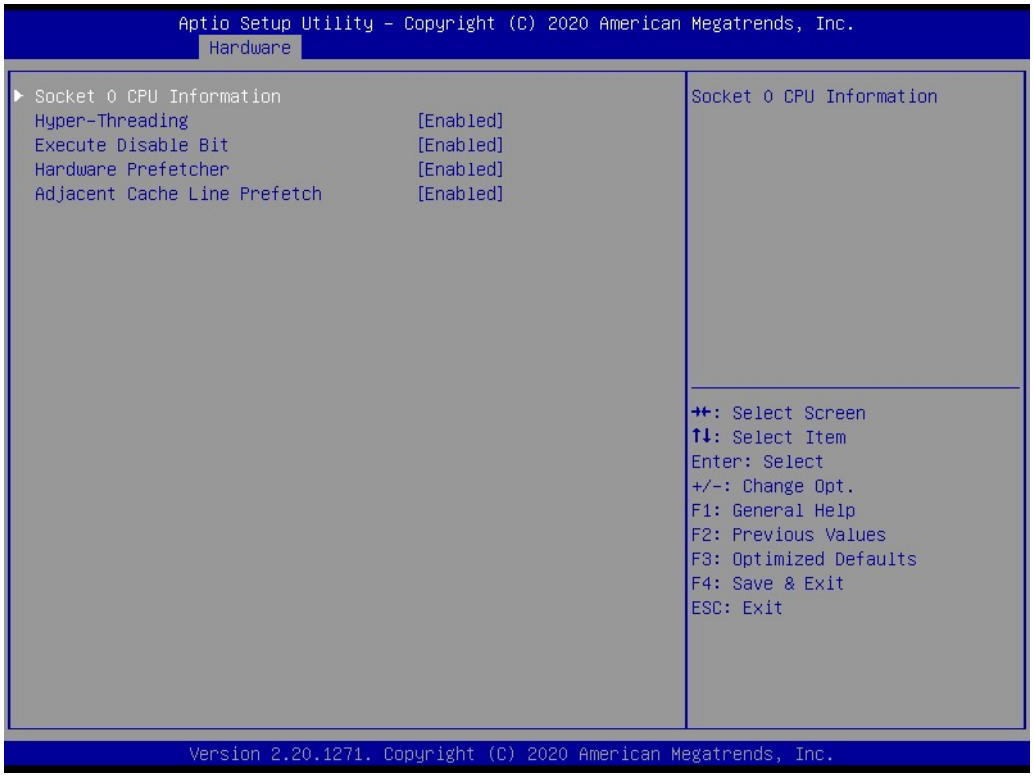


Figure 2.12 CPU Configuration

- **Hyper-Threading**
  This item allows users to enable/disable the CPU hyper-threading function. The default setting is enabled for Windows XP and Linux (OS optimized for hyper-threading technology) and disabled for other OS (OS is not optimized for hyper-threading technology).
- **Execute Disable Bit**
  XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS. (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, RedHat Enterprise 3 Update 3.)
- **Hardware Prefetcher**
  This item allows users to enable/disable the MLC streamer prefetcher.
- **Adjacent Cache Line Prefetch**
  This item allows users to enable/disable the prefetching of adjacent cache lines.

2.3.3.2 Northbridge

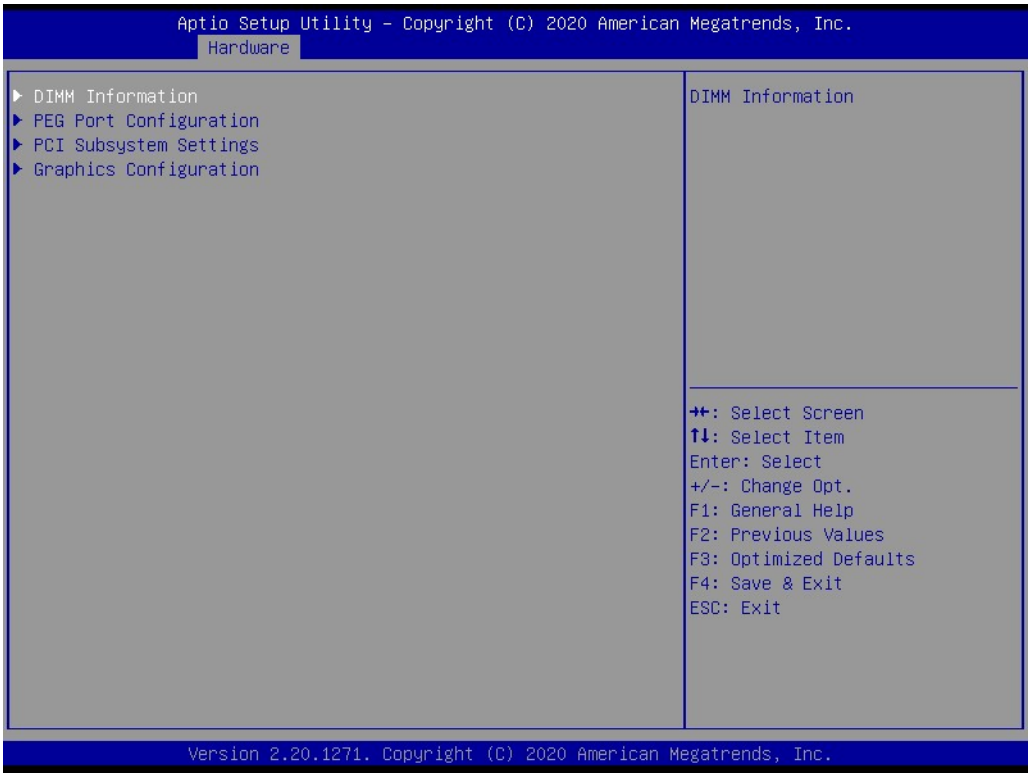


Figure 2.13 Northbridge

2.3.3.3 Memory Configuration

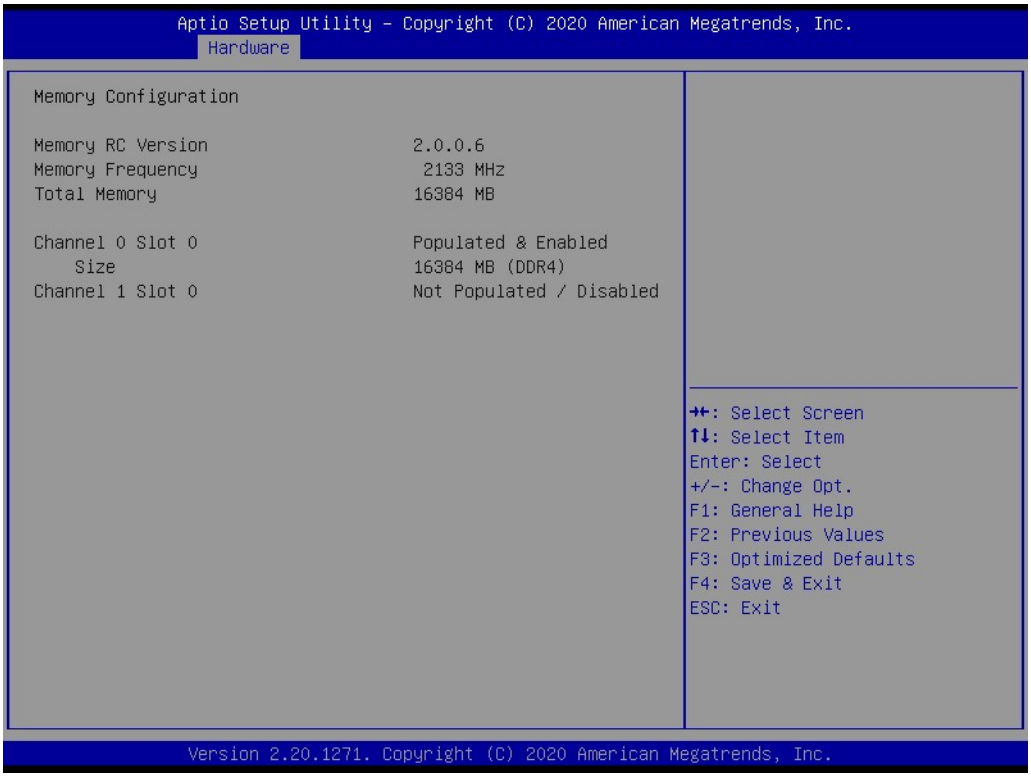


Figure 2.14 Memory Configuration

This page shows the memory information.

2.3.3.4 PEG Port Configuration

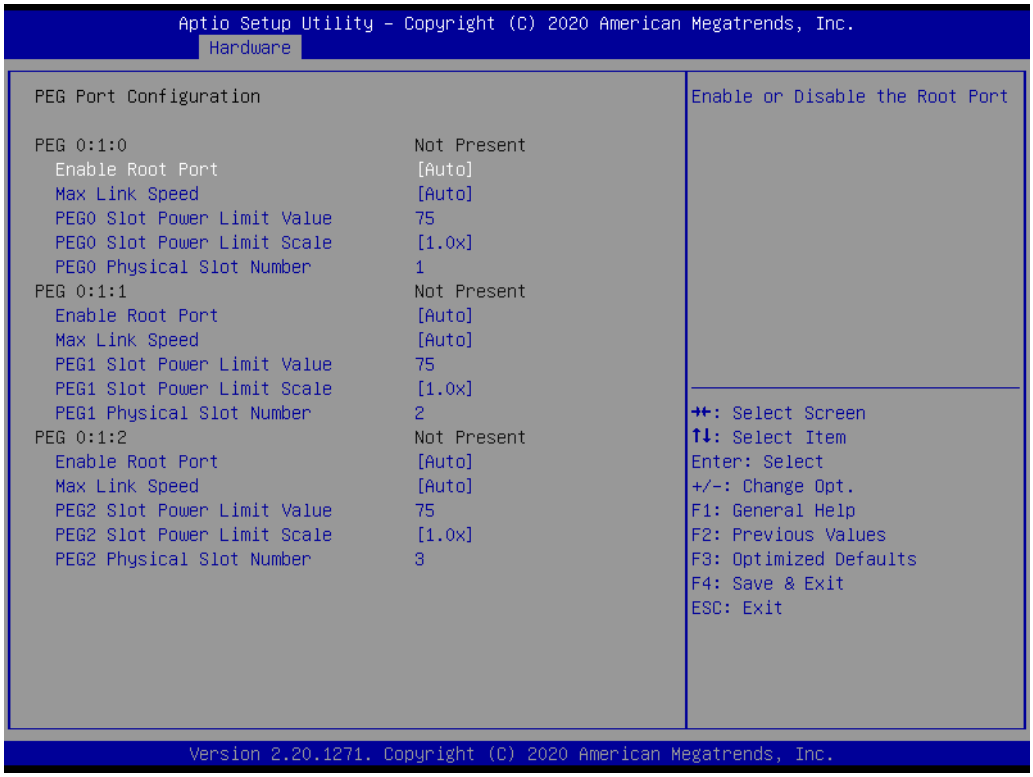


Figure 2.15 PEG Port Configuration

- **Enable Root Port**
  This item allows users to enable/disable the root port.
- **Max Link Speed**
  This item allows users to configure PEG 0:1:0 /0:1:1/0:1:2 max. speed.
- **PEG0/1/2 Slot Power Limit Value**
  This item allows users to set the upper limit of power supplied by the slot. Power limit (Watts) is calculated by multiplying this value by the slot power limit scale. Values 0 - 255.
- **PEG0/1/2 Slot Power Limit Scale**
  This item allows users to select the scale used for the slot power limit value.
- **PEG0 Physical Slot Number**
  This item allows users to set the physical slot number attached to this port. The number must be globally unique within the chassis. Values 0 - 8191.
  NOTE: When the mode is switched to 2x8 PCI Express, the two PCI Express slots correspond to PEG0 and PEG1. When switched to 1 x8 and 2 x4 PCI Express, the three PCI Express slots correspond to PEG0, PEG1, and PEG2.

2.3.3.5 PCI Subsystem Settings

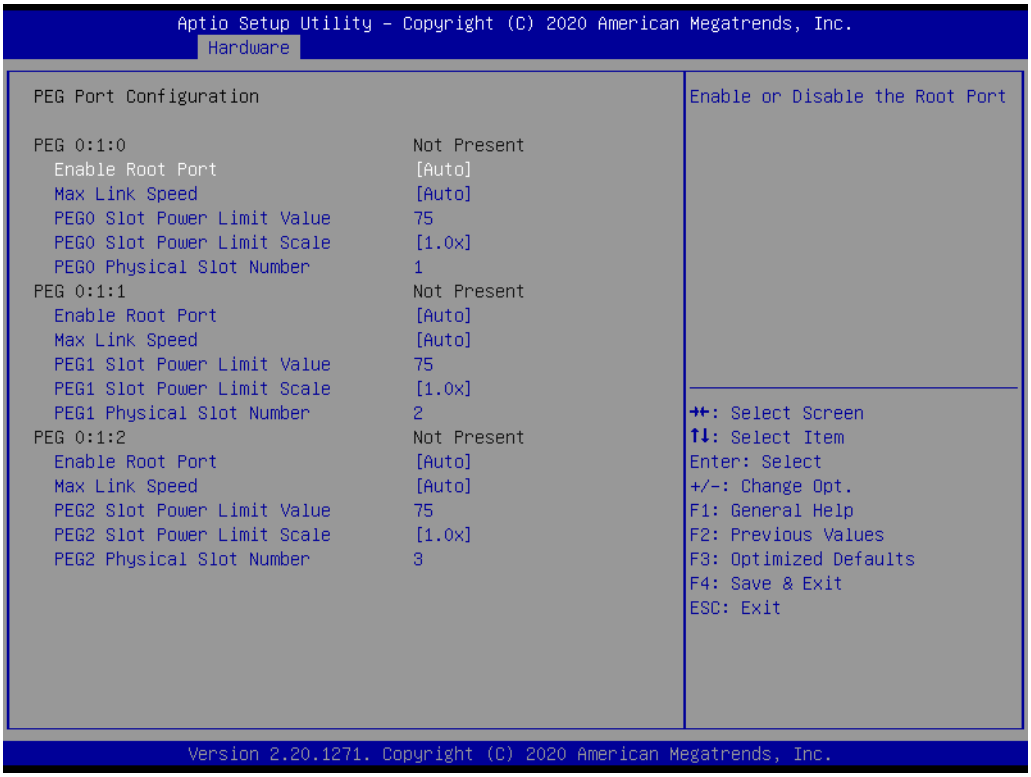


Figure 2.16 PCI Subsystem

- **Above 4G Decoding**
  This item allows users to enable/disable the decoding of 64-bit-capable devices in above 4G address space (this option is only available is the system supports 64-bit PCI decoding).

2.3.3.6 Graphics Configuration

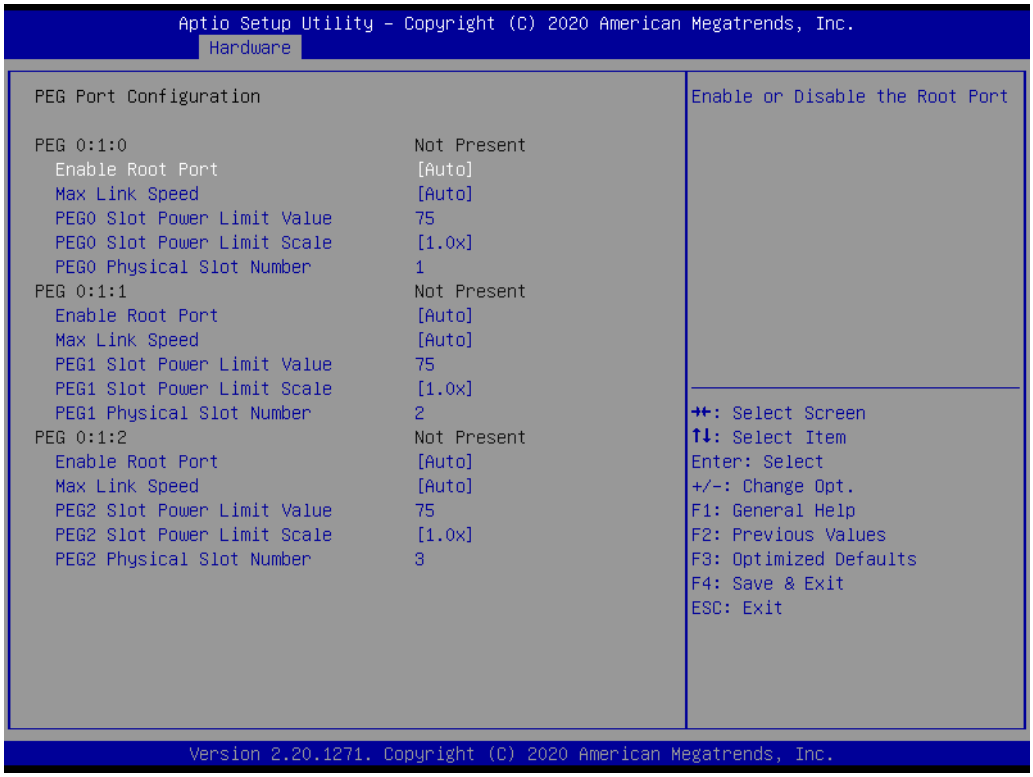


Figure 2.17 Graphics Configuration

- **Primary Display**
  This item allows users to select which of the IGFX/PEG/PCI graphics device should be the primary display, or select SG for switchable GFX.
- **Internal Graphics**
  This item allows users to keep IGFX enabled based on the setup options.
- **GTT Size**
  This item allows users to select the GTT size.
- **Aperture Size**
  This item allows users to select the aperture size.
  NOTE: Above 4GB MMIO BIOS assignment is automatically enabled when selecting 2048 MB aperture. To use this feature, disable CSM support.
- **DVMT Pre-Allocated**
  This item allows users to select the DVMT 5.0 pre-allocated (fixed) graphics memory size used by the internal graphics device.
- **DVMT Total Gfx Mem**
  This item allows users to select the DVMT5.0 total graphics memory size used by the internal graphics device.

2.3.3.7 LCD Control

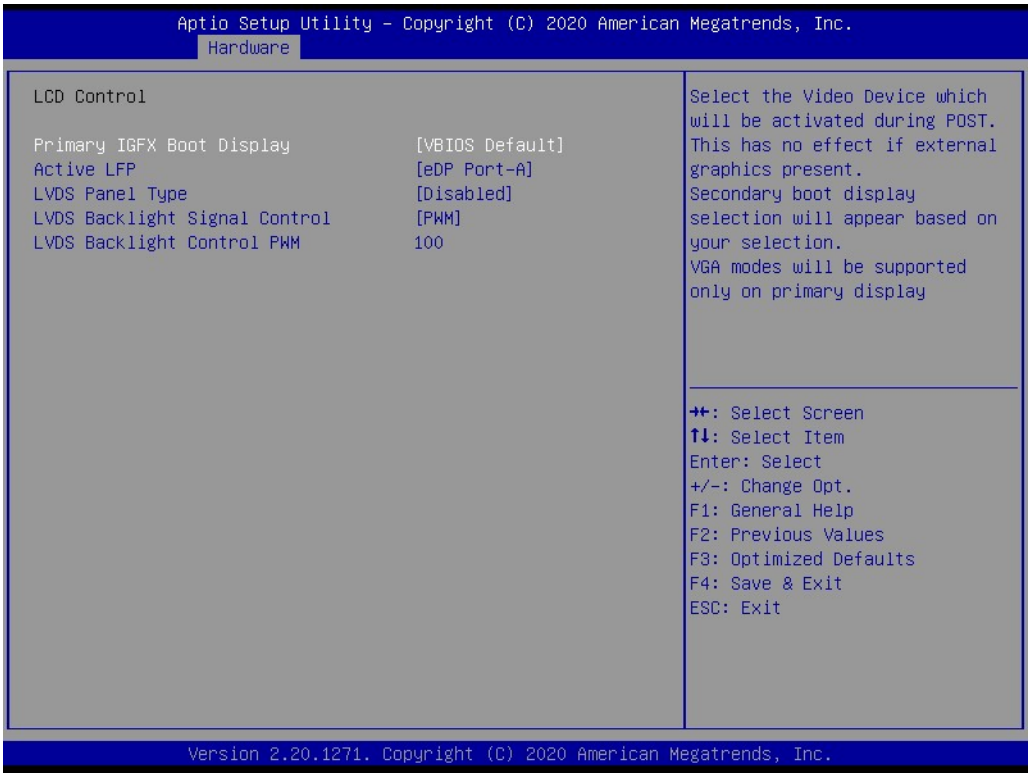


Figure 2.18 LCD Control

- **Primary IGFX Boot Display**
  This item allows users to select the video devices to be activated during POST. This has no effect if external graphics are present. Secondary boot display options will appear based on your selection. VGA modes are supported only on the primary display.
- **Active LFP**
  This item allows users to set the Active LFP configuration settings.
  No LVDS: VBIOS does not enable LVDS.
  Int-LVDS: VBIOS enables the LVDS driver via the integrated encoder.
  SDVO LVDS: VBIOS enables the LVDS driver via the SDVO encoder.
  eDP Port-A: LFP driven by the internal DisplayPort encoder from Port-A.
- **LVDS Panel Type**
  This item allows users to select the LVDS panel type.
- **LVDS Backlight Signal Control**
  This item allows users to configure the LVDS backlight signal as PWM or linear.
- **LVDS Backlight Control PWM**
  This item allows users to configure the expected PWM output value (Range: 0 - 100%).

2.3.3.8 Southbridge

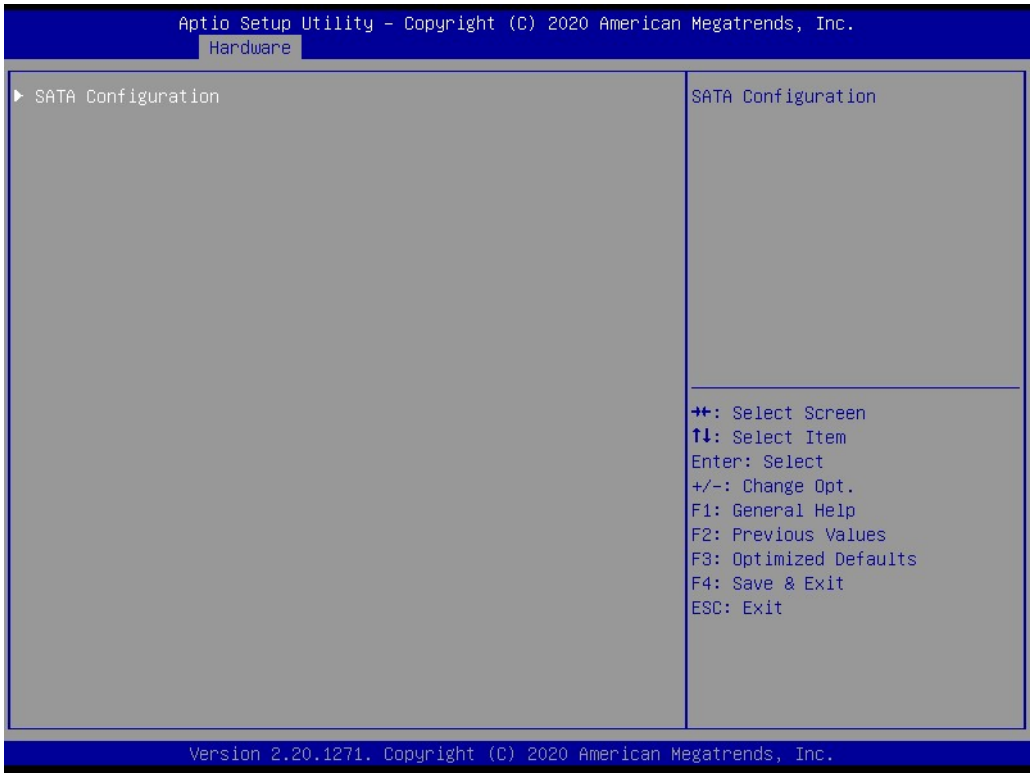


Figure 2.19 Southbridge

2.3.3.9 SATA Configuration

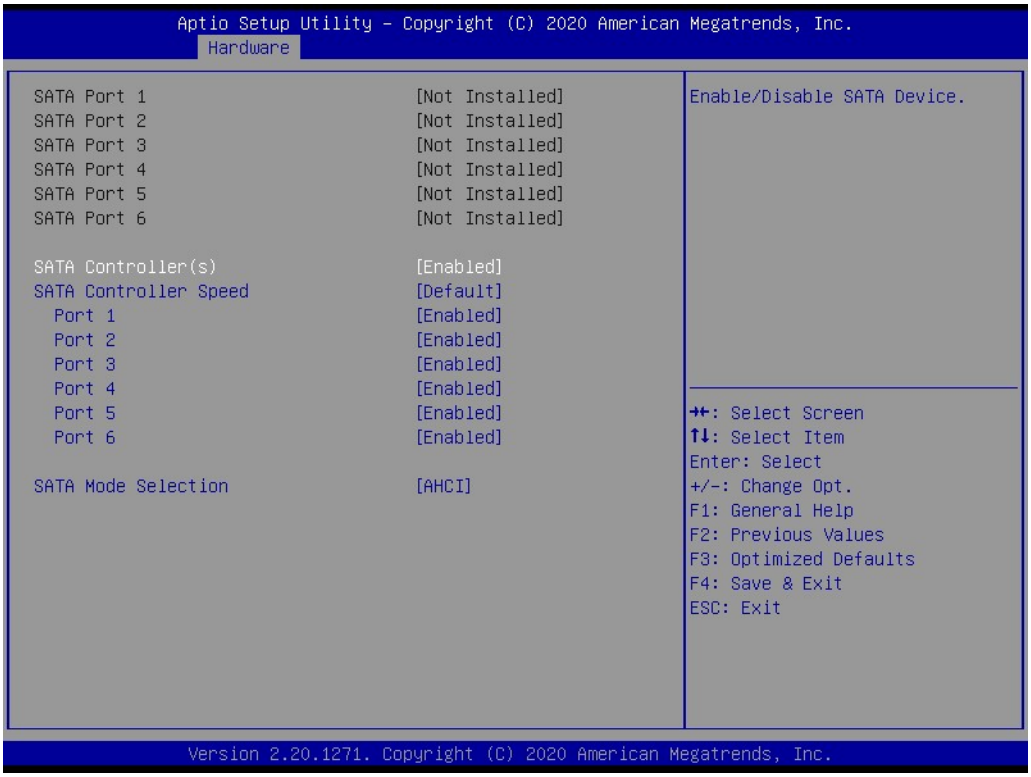


Figure 2.20 SATA Configuration

- **SATA Controller(s)**
  This item allows users to enable/disable SATA devices.
- **SATA Controller Speed**
  This item allows users to configure the maximum speed the SATA controller can support and to enable/disable SATA port 1/port 2/port 3/port 4/port 5/port 6.
- **SATA Mode Selection**
  This item allows users to configure the SATA controller(s) operation mode.

2.3.3.10 NCT6126D Super I/O Configuration

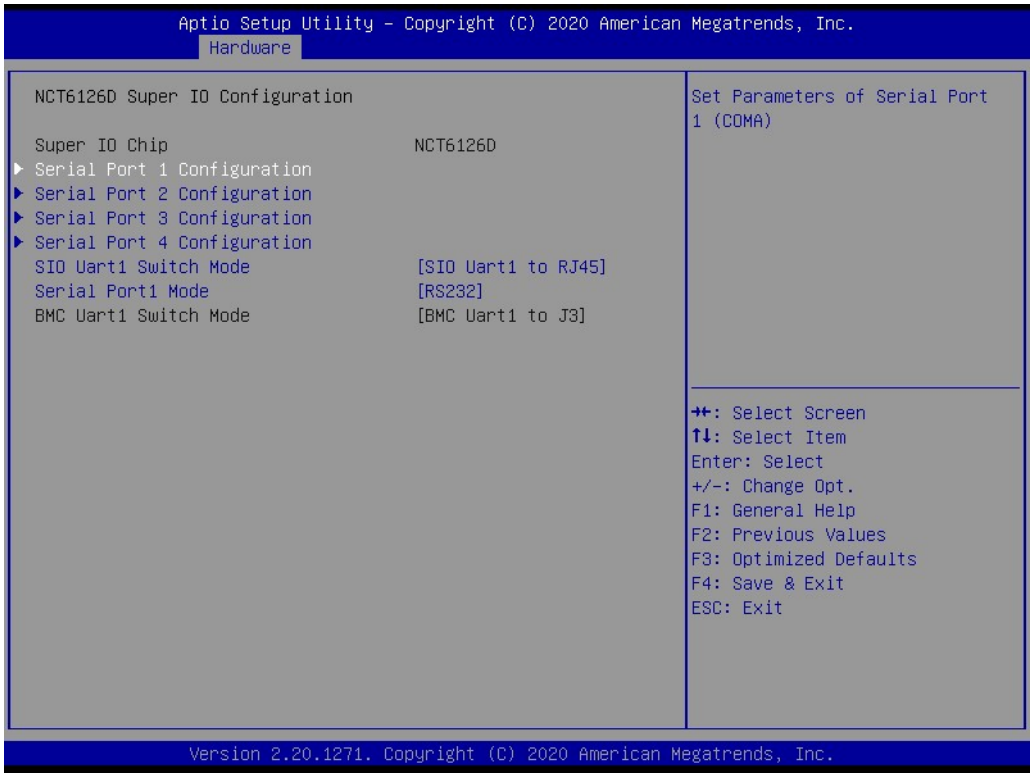


Figure 2.21 NCT6126D Super I/O Configuration

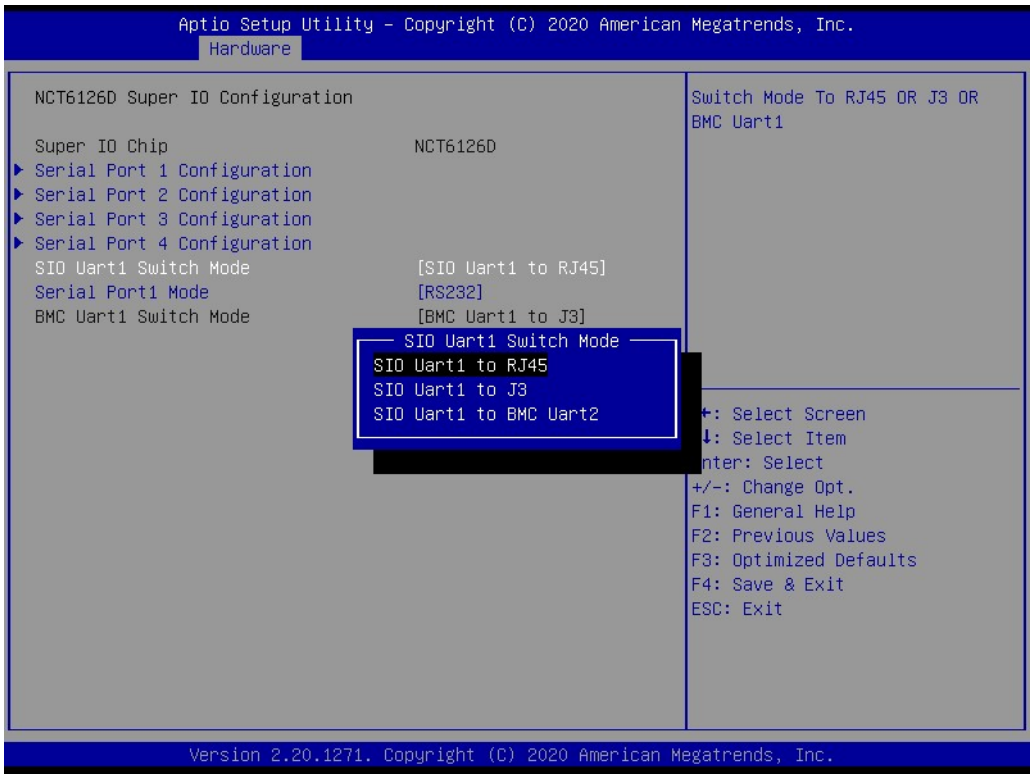


Figure 2.22 SIO Uart1 to RJ45

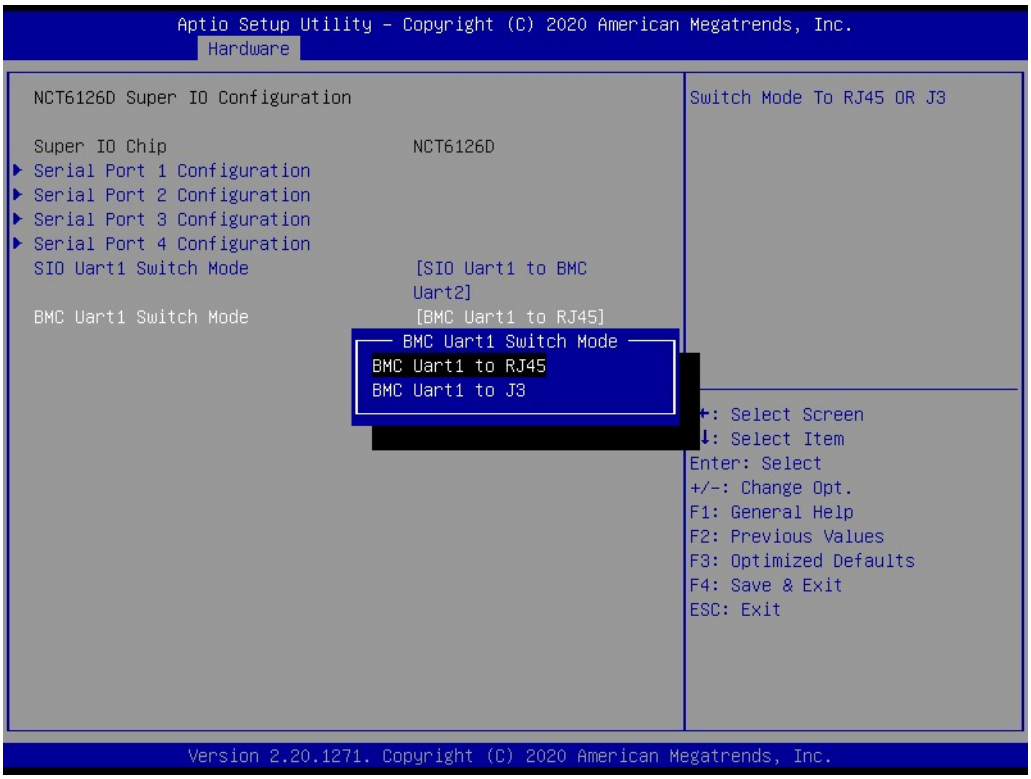


Figure 2.23 SIO UART1 to BMC UART2

- **SIO Uart1 Switch Mode**
  This item allows users to switch the SIO Uart1 mode to front I/O RJ45, J3, or BMC Uart1.
  When SIO Uart1-to-RJ45 is selected, the BMC Uart1 switch mode will be set to J3 automatically. When SIO Uart1-to-BMC J3 is selected, the BMC Uart1 switch mode will be set to RJ45 automatically. When SIO UART1-to-BMC Uart2 is selected, the BMC Uart1 switch can be set to RJ45 or J3.

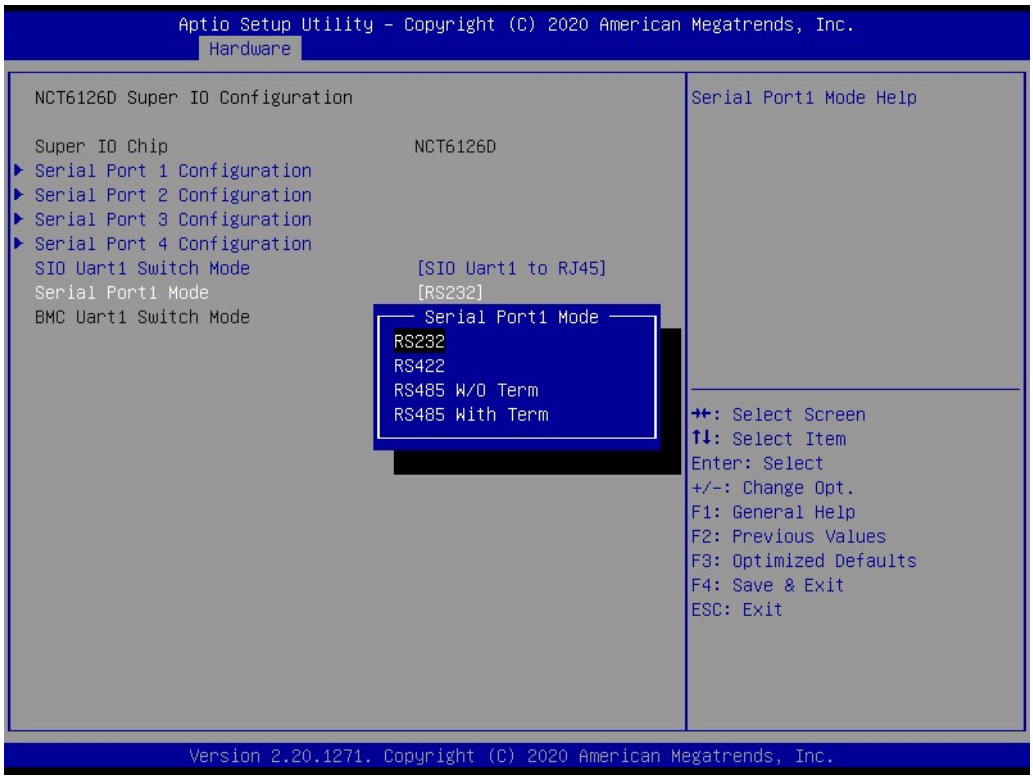


Figure 2.24 Serial Port Mode

- **Serial Port1 Mode**
  This item allows users to set the serial port1 mode as RS-232, RS-422, or RS-485.

2.3.3.11 Serial Port 1 Configuration

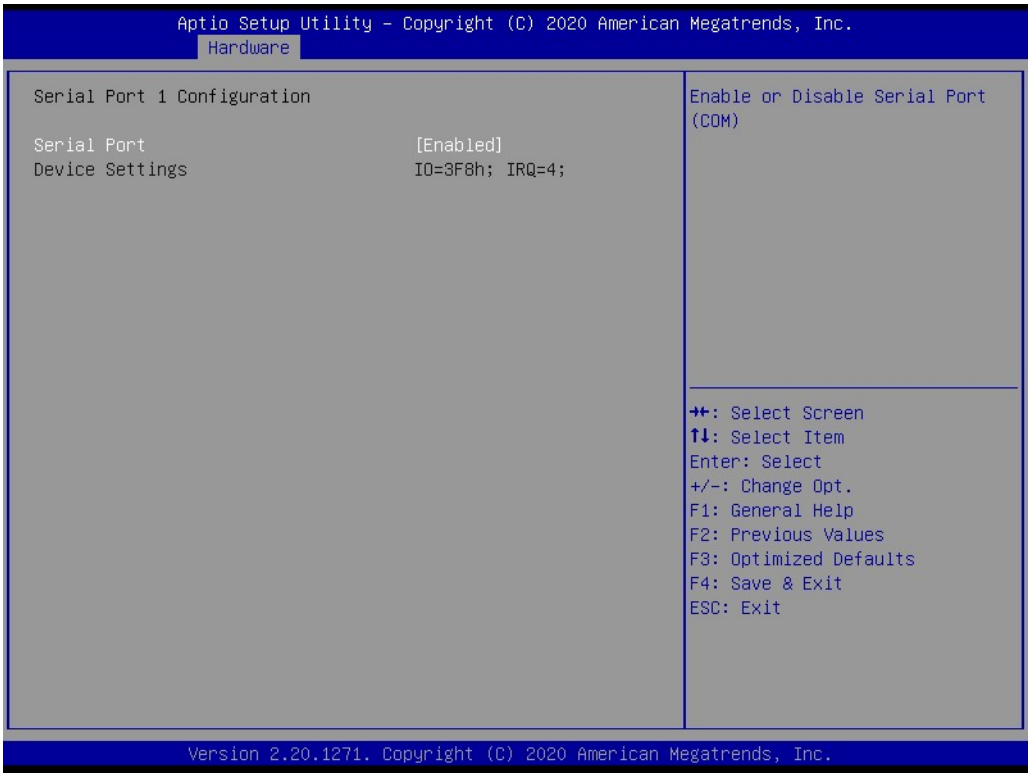


Figure 2.25 Serial Port1 Configuration

- **Serial Port**
  This item allows users to enable/disable the serial port (COM).

2.3.3.12 Serial Port 2 Configuration

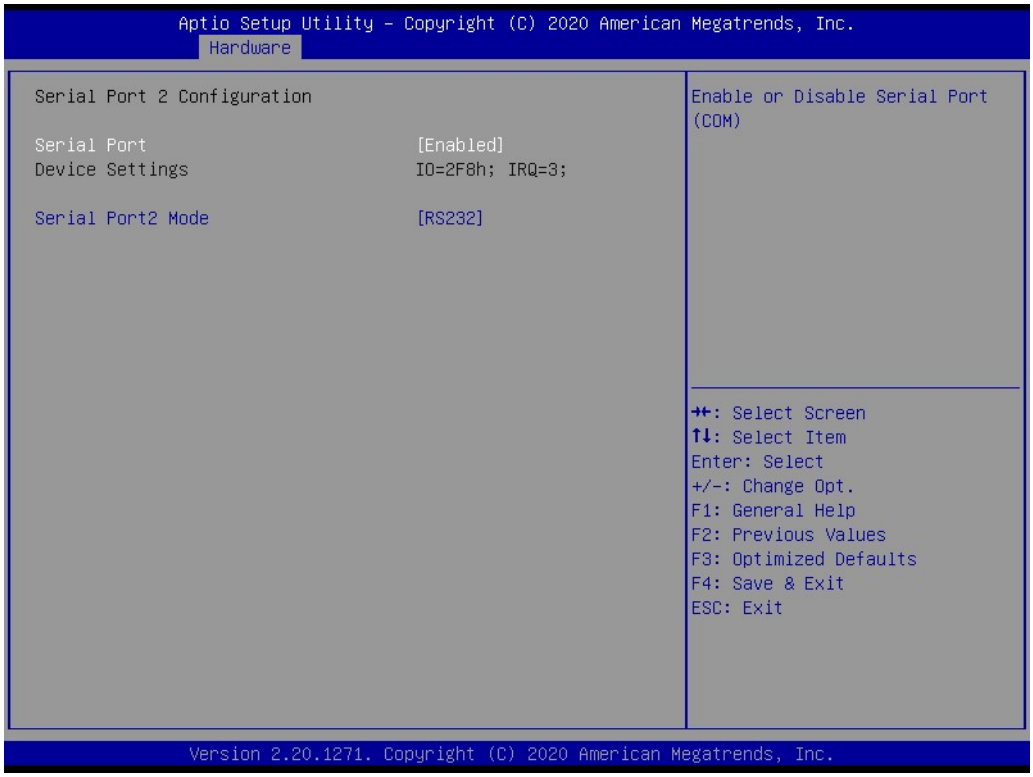


Figure 2.26 Serial Port 2 Configuration

- **Serial Port**
  This item allows users to enable/disable the serial port (COM).
- **Serial Port2 Mode**
  This item allows users to set the serial Port2 mode as RS-232, RS-422, RS-485 without term, or RS-485 with term.

2.3.3.13 Serial Port 3 Configuration

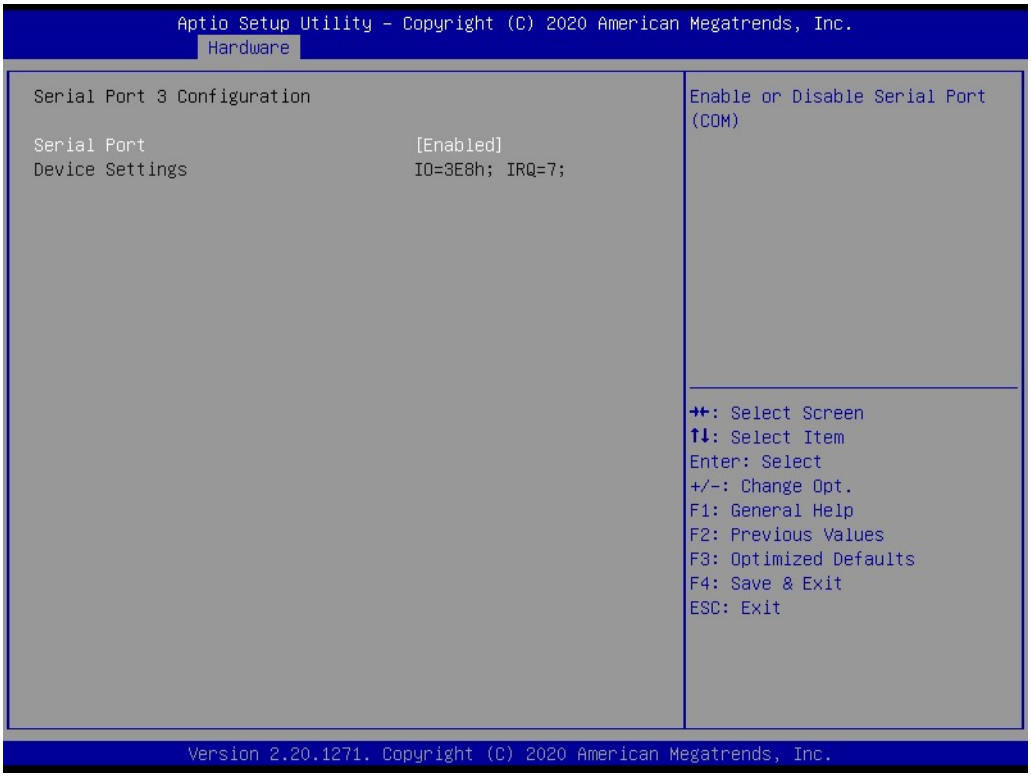


Figure 2.27 Serial Port 3 Configuration

- **Serial Port**
  This item allows users to enable/disable the serial port (COM).

2.3.3.14 Serial Port 4 Configuration

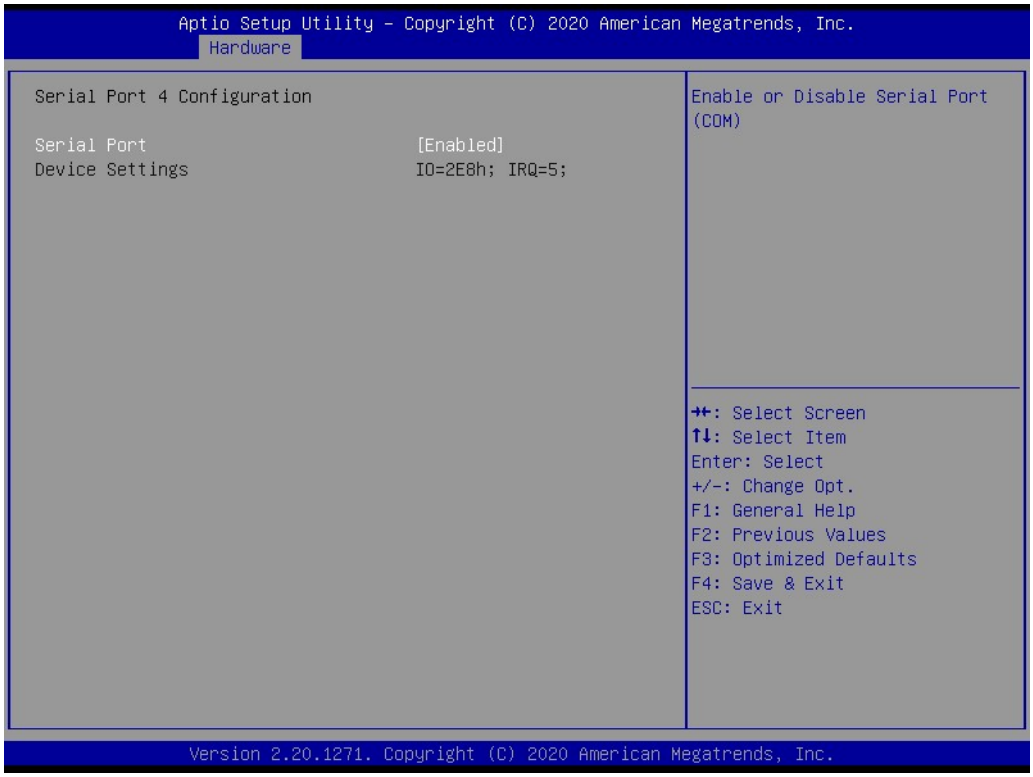


Figure 2.28 Serial Port 4 Configuration

- **Serial Port**
  This item allows users to enable/disable the serial port (COM).

2.3.3.15 H/W Monitor Configuration

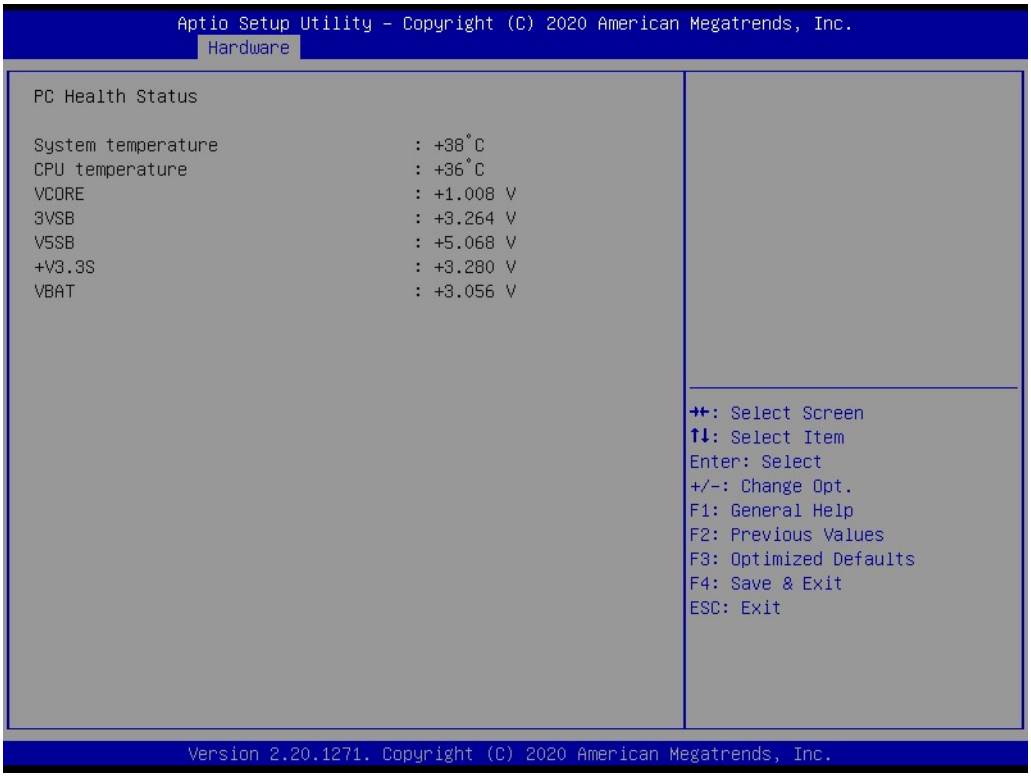


Figure 2.29 H/W Monitor configuration

This page shows the PC heath status information.

2.3.4 Server Management

Click the Server Mgmt tab to enter the Server Mgmt setup menu. Users can select any item in the left frame of the screen to access the submenu for that item. The Server Mgmt tab is only available for motherboards with BMC.

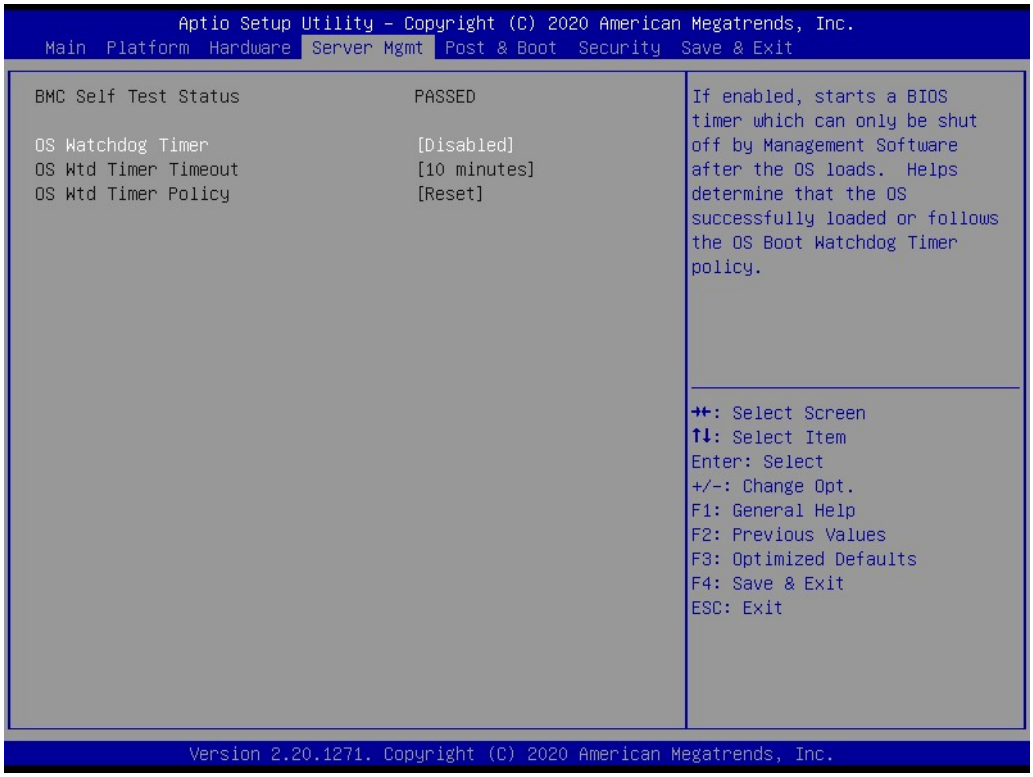


Figure 2.30 Server Mgmt BIOS Setup Page

- **OS Watchdog Timer**
  This item allows users to enable/disable the OS watchdog timer. If enabled, the system will start a BIOS timer that can only be shut off by management software after the OS loads. The OS watchdog timer helps determine whether the OS has successfully loaded or follows the OS boot watchdog timer policy.
- **OS Wtd Timer Timeout**
  This item allows users to configure the timeout period of the OS boot watchdog timer. This option is not available if the OS boot watchdog timer is disabled.
- **OS Wtd Timer Policy**
  This item allows users to configure the system response when the OS boot watchdog time expires. This option is not available if the OS boot watchdog timer is disabled.

2.3.5 Post & Boot

Select the Post & Boot tab to enter the Post & Boot setup page. Users can select any item in the left frame of the screen to access the submenu for that item.

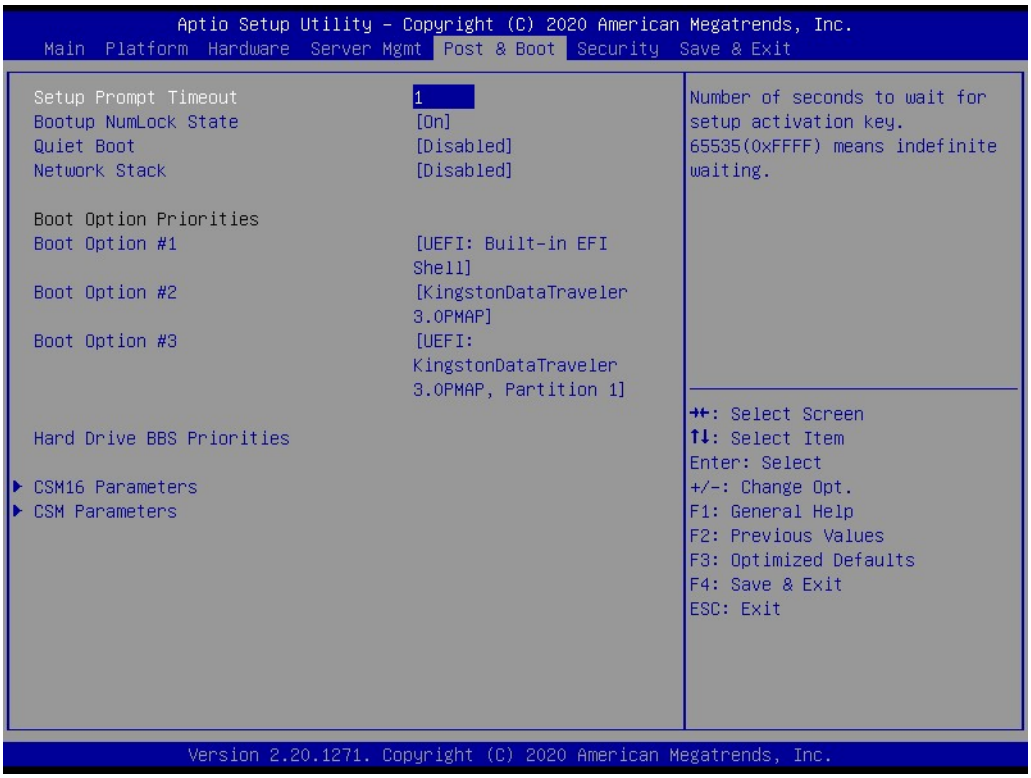


Figure 2.31 Post & Boot BIOS Setup Page

- **Setup Prompt Timeout**
  This item allows users to configure the number of seconds to wait for a setup activation key. 65535 (oxFFFF) means indefinite waiting.
- **Boot Up NumLock State**
  This item allows users to select the keyboard numlock state. When set to on, the keyboard numlock state will stay on after booting. When set to off, the keyboard numlock state will stay off after booting.
- **Quiet Boot**
  This item allows users to enable/disable the quiet boot option. If this option is disabled, the BIOS will display normal POST messages. If enabled, an OEM logo will be displayed instead of POST messages.
- **Network Stack**
  This item allows users to enable/disable the UEFI network stack.
- **Boot Option**
  This item allows users to view the boot priority of devices.
  Boot Option #1
  Boot Option #2
  Boot Option #3
- **Hard Drive BBS Priorities**
  This item allows users to set the boot device priority sequence from the available hard disk drives.

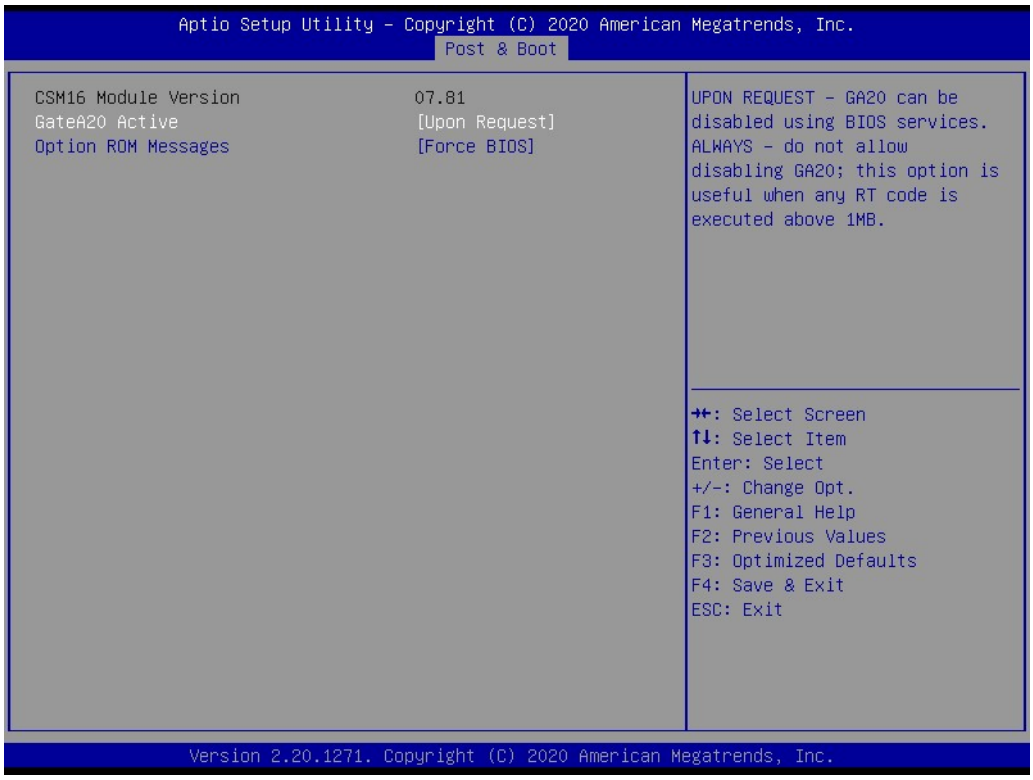


Figure 2.32 CSM16 Parameters

- **CSM16 Parameters**
  This item allows users to set the display mode for option ROM.
- **GateA20 Active**
  This item allows users to enable/disable GA20 active status. This option is useful when any RT code is executed above 1 MB. When configured as upon request, GA20 can be disabled using the BIOS. When configured as always, GA20 disabling is not allowed.

2.3.5.1 CSM Parameters

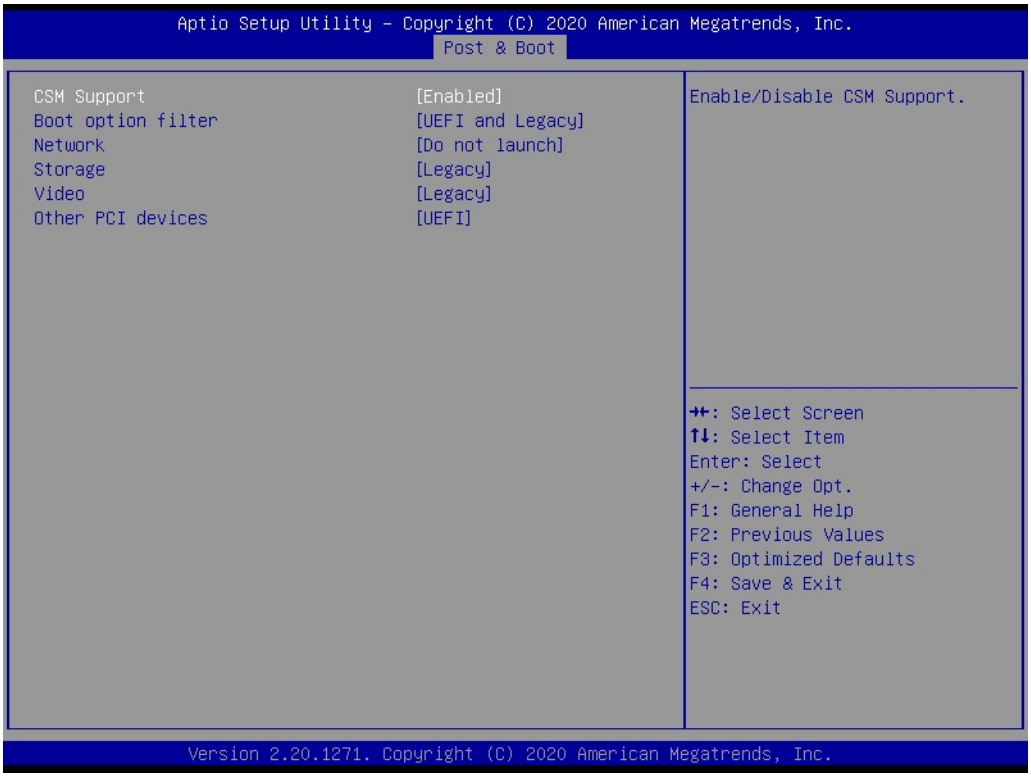


Figure 2.33 CSM Parameters

- **CSM Support**
  This item allows users to enable/disable CSM support.
- **Boot Option Filter**
  This item allows users to configure the legacy/UEFI ROMs priority.
- **Network**
  This item allows users to configure the execution of the UEFI and legacy PXE option.
- **Storage**
  This item allows users to configure the execution of the UEFI and legacy storage OpROM.
- **Video**
  This item allows users to configure the execution of the UEFI and legacy video OpROM.
- **Other PCI Devices**
  This item allows users to configure the OpROM execution policy for devices other than Network, Storage, or Video.

2.3.6 Security

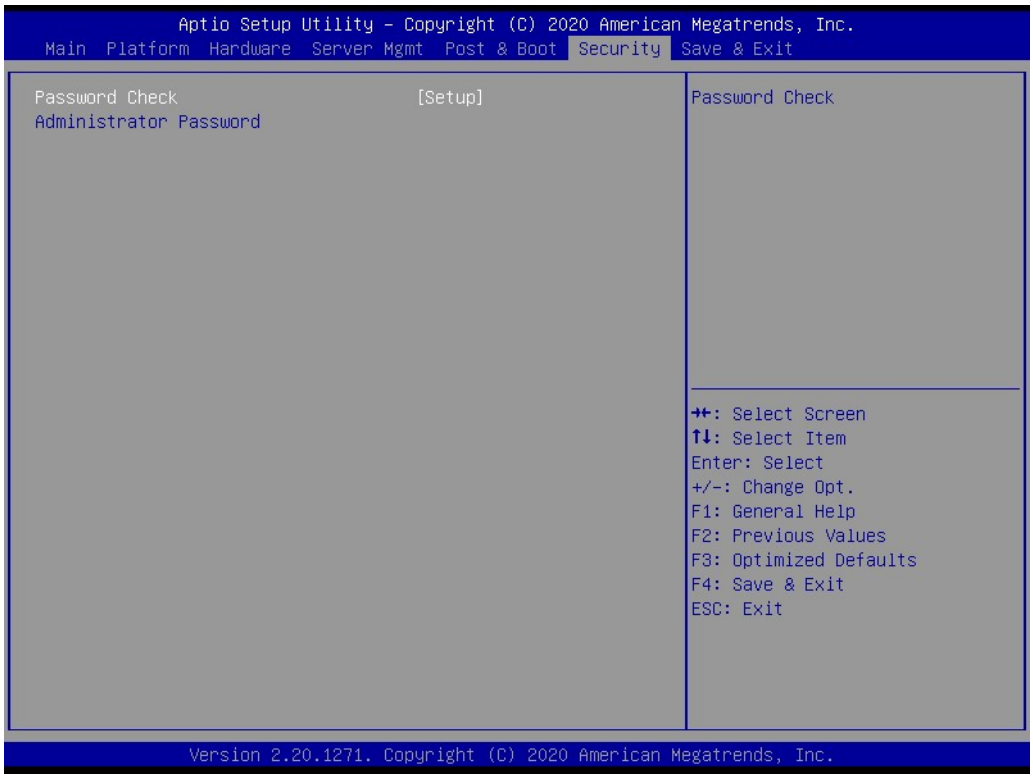


Figure 2.34 Security Settings

- **Password Check**
  - Password Check: Set password check mode.
  - Administrator Password: Set administrator password.

2.3.7 Save & Exit

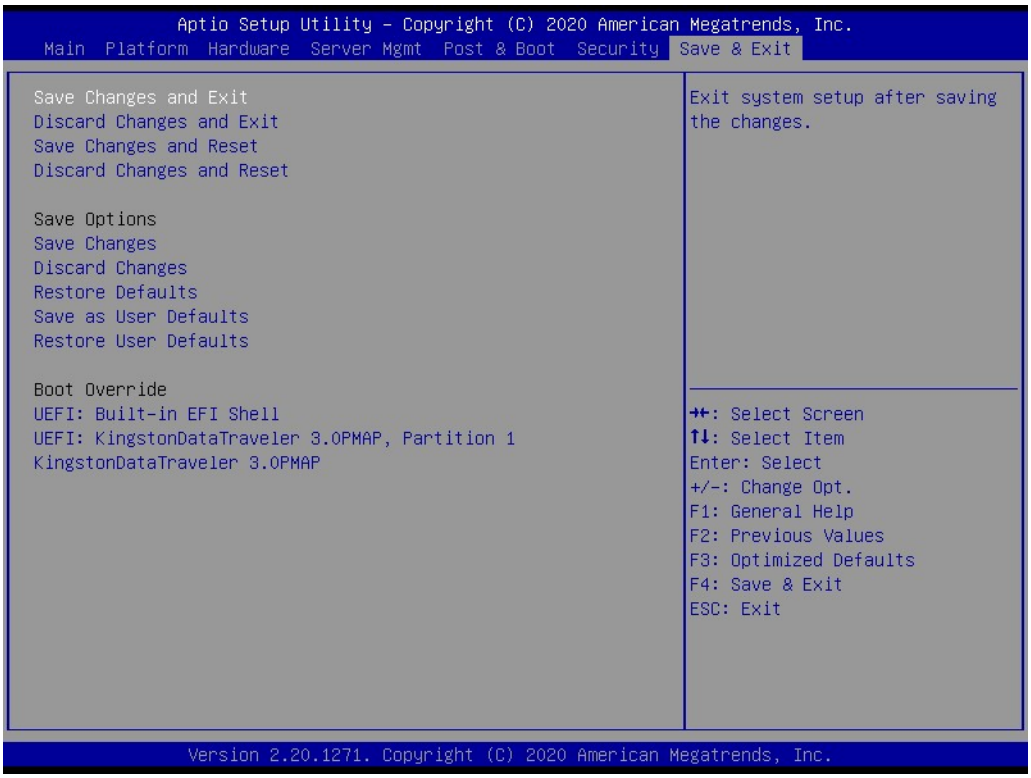


Figure 2.35 Save & Exit

- **Save Changes and Exit**
  This item allows users to exit the BIOS utility after saving all changes. The system must be rebooted for the configuration changes to take effect.
- **Discard Changes and Exit**
  This item allows users to exit the BIOS utility without saving any changes.
- **Restore Default**
  This item allows users to restore the default values for the setup options. The BIOS automatically configures all setup items to optimal settings when users select this option. Defaults are designed for maximum system performance, but may not work best for all computer applications. Do not use default settings if the computer is experiencing configuration problems.
- **Save as User Default**
  This item allows users to save all current settings as user defaults.
- **Restore User Default**
  This item allows users to restore all settings to the user defaults.
- **Boot Override**
  This item allows users to select the device to boot.

Chapter 3

IPMI Configuration

This chapter describes IPMI configuration for MIC-3399.

3.1 Introduction

MIC-3399 supports the IPMI 2.0 interface and PICMG 2.9 R1.0 specification. The BMC solution is based on Advantech IPMI Core G02 and is designed around a combination of an NXP LPC1768 ARM Cortex-M3-based 32-bit microcontroller and a Lattice MachXO2 series FPGA.

The microcontroller is running FreeRTOS as the basic OS, with Advantech's own hardware abstraction layer (HAL) and IPMI stack.

The BMC's key features and functions are listed below.

Advantech Integrity Sensor

Based on the Advantech IPMI core and designed for CompactPCI.

- IPMI 2.0 compliant
- IPMI-over-LAN
- Serial-over-LAN
- KCS interface for direct IPMI communication between the OS and BMC
- Full BMC watchdog support as defined in the IPMI specification
- System event log (SEL)
- HPM.1 for in-field updates supports:
  - Bootloader
  - Firmware
  - FPGA
  - BIOS
- Automatic UART muxing between all serial interfaces for easy console access
- Additional sensors for hardware monitoring

3.2 Terms and Definitions

Term	Definition
AMC	Advanced mezzanine card
API	Application programming interface
ATCA	Advanced telecommunications computing architecture
BIOS	Basic input/output system
BMC	Baseboard management controller
CLI	Command line interface
CPCI	CompactPCI
CPU	Central processing unit
DDR4	Double data rate 4
DIMM	Dual in-line memory module
DIP	Dual in-line package
FLASH	Flash memory
FPGA	Field-programmable gate array
FRU	Field-replaceable unit
GbE	Gigabit Ethernet
GPIO	General purpose input/output
HPM.1	Hardware platform management.1
I2C	Inter integrated circuit
IPMB	Intelligent platform management bus
IPMI	Intelligent platform management interface
KCS	Keyboard controller style
LPC	Low pin count (bus)
NCSI	Network controller sideband interface
NIC	Network interface controller
RMCP	Remote management communication protocol
RS-232	Recommended standard 232
SAS	Serial attached storage
SATA	Serial advanced technology attachment
SDR	Sensor data record
SEL	System event log
SPI	Serial peripheral interface
UART	Universal asynchronous receiver transmitter
USB	Universal serial bus
XMC	XMC mezzanine card (Vita 42.0)

3.3 IPMI Interfaces

MIC-3399 provides three main IPMI messaging interfaces to connect to the BMC. There is the IPMB-0 main messaging interface between CPCI boards, the LAN-side band interface (NCSI), and the on-board payload interface to x86 (KCS).

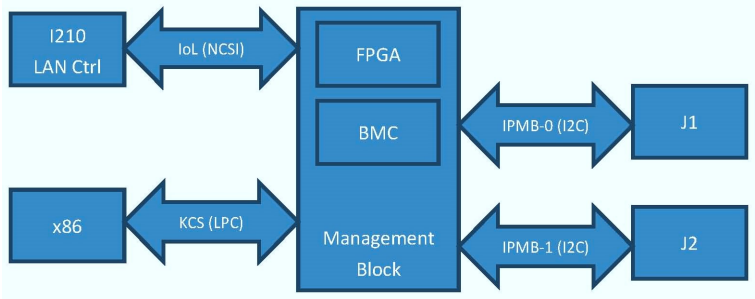


Figure 3.1 Management Block Diagram

3.3.1 IPMB-0

IPMB-0 is the I2C-based PICMG 2.9 R1.0-defined main messaging interface between CPCI boards. It consists of one I2C bus clocked at a frequency of 100 kHz, using IPMI-compliant messaging.

3.3.2 KCS

The BMC KCS interface is implemented according to the IPMI 2.0 specification. Keyboard controller style (KCS) interfacing describes a legacy system interface based around a bidirectional set of status/command and data register.

This type of interface has been adopted as the IPMI system interface and provides the following benefits:

- Higher bandwidth than that of I2C or RS-232-based interfaces
- Robustness
- Auto-discovery options

3.3.3 LAN

The BMC firmware supports a LAN interface, providing RMCP/RMCP+ according to the IPMI 2.0 specification.

The table below lists the supported network protocols.

Table 3.1: Supported Network Protocols

Mnemonic	Protocol
ARP	Address Resolution Protocol
ICMP	Internet Control Message Protocol
IP	Internet Protocol
UDP	User Datagram Protocol
RMCP/RMCP+	Remote Management Control Protocol

3.3.3.1 ARP

Both standard ARP requests and responses (ARP opcodes 0x01 and 0x02) are supported to propagate the BMC's IP address in the system. Gratuitous ARP is supported for dynamic address changes or failover scenarios. Other ARP opcodes are not supported and will be ignored.

3.3.3.2 ICMP

ICMP is supported to allow network pings to/from the BMC.

3.3.3.3 RMCP/RMCP+

IPMI-over-LAN (IOL) uses RMCP as the messaging protocol, as defined in the IPMI specifications. RMCP messages consist of the basic IPMI message with some RMCP-specific overhead and use the UDP protocol for data transmissions.

UDP uses the IP protocol for data transmissions. Thus, the network stack must support the IP and UDP protocols along with RMCP.

RMCP+ was added in the IPMI v2.0 specification. It is an enhanced protocol for transferring IPMI messages and other types of payloads (e.g., serial data).

3.4 Command Line Interface

In addition to the IPMI-defined interfaces, the Advantech IPMI core supports a command line interface to provide rapid and easily readable system information. This can be used for debugging and error recovery as well as showing the board information and firmware status. The command line interface (CLI) is implemented on UART 0 and accepts high level commands as well as IPMI messages in Serial Terminal Mode, as specified in IPMI 1.5.

The CLI uses a baud rate of 115200, 8 data bits, 1 stop bit, and no parity.

Table 3.2: Standard CLI Commands

Command	Description
[…]	Any value between this bracket will be interpreted as an IPMI message
<Enter>	Confirm input
<Up>	Step through history
bios_hist	Show BIOS POST code history
cpci_payload	Get CPCI payload power status
date	Display current date and time
debug	Enable and select debug options
help	Print command overview
info	Print firmware and product information
ip	Set controller IP address
defgw	Set controller default gateway address
ncsi_Set	Set ncsi behavior
ncsi_status	Print detailed NC-SI status
ncsi_table	Print NC-SI link status table
pch_temp	PCH temperature read via SMBus
peci_get_dib	CPU PECI-get device info and revision number
peci_rd_cpu_pci	CPU PECI-read internal PCI configuration
peci_rd_iamsr	CPU PECI-read IA model specific register
peci_rd_pkg	CPU PECI-read package configuration
peci_rd_pci	CPU PECI-read external PCI configuration
peci_wr_pkg	CPU PECI-write package configuration
reboot	Reboot
sel	Print system event log
sensor	Show device sensors
spidump	Dump all FPGA SPI registers

3.5 BMC Watchdog

The BMC provides an IPMI 2.0-compliant BMC watchdog to monitor the OS during runtime or to observe the BIOS boot progress.

3.5.1 BIOS Boot Watchdog

The IPMI-compliant BMC watchdog is used to monitor BIOS boot progress and initiate a rollback when a BIOS is found to be corrupt.

It is set to a predefined value of 180 seconds and automatically starts when the payload power for the x86 subsystem is turned on. The timeout action is set to “hardware reset”, with the timer use indicating BIOS use.

If the watchdog timer times out with this configuration, it triggers a BIOS chip failover followed by a system reset and restart of the watchdog timer. The mechanism runs in an endless loop and logs timeouts + failovers to the SEL through the integrity sensor.

BIOS does not modify the watchdog timer except for two situations:

- It disables the watchdog right before jumping into the boot loader to avoid triggering after BIOS execution. It can alternatively reconfigure the watchdog to act as a boot watchdog (i.e., change the timeout action).
- It temporarily disables the watchdog once the setup menu is manually activated for debugging purposes.

3.6 System Event Log (SEL)

A 64-KB SEL is implemented in the BMC. It stores all events that are either generated by the BMC or that are passed to it from the system interface. The events are physically stored in the externally attached SPI flash.

All received events are passed to the default event receiver (which is typically the CMM in PICMG2.9 environments if one is present), regardless of whether it is stored in the SEL. This means that local events will show up in the local BMC’s SEL as well as in the CMMs shelf-wide SEL, unless there is no filter enabled on the CMM side.

The 64 KB size is sufficient to hold exactly 4096 entries of 16 bytes each.

3.7 Sensors

All important voltages and temperatures are connected to the BMC management system in different ways.

Moreover, the BMC also registers several logical, discrete sensors as listed below.

- BMC watchdog sensor
- FW progress sensor
- Version change sensor
- Advantech OEM sensor: integrity sensor

3.7.1 Sensor List

All sensors provided by the BMC are listed in the table below.

Table 3.3: BMC Sensor List

No.	Sensor ID	Sensor Type	Description
0	MIC-3399	-	IPMI FRU Device Locator
1	IPMB_0	F1h/6Fh	PICMG IPMB-0 status sensor
2	BMC_HEALTH	28h/6Fh	IPMI Management Subsystem Health
3	VERSION_CHANGE	2Bh/6Fh	IPMI Version Change sensor
4	BMC_WATCHDOG	23h/6Fh	IPMI BMC Watchdog sensor
5	ACPI_STATE	22h/6Fh	IPMI System ACPI Power State sensor
6	PROC_STATE	07h/6Fh	IPMI Processor sensor
7	SYSTEM_RESET	1Dh/6Fh	Payload system reset indication
8	FW_PROGRESS	0Fh/6Fh	IPMI FW Progress sensor
9	INTEGRITY	C0h/70h	Advantech Integrity OEM sensor
10	POWER_GOOD	08h/6Fh	IPMI Power Supply sensor
11	HOT_5_0-VOL	02h/01h	Standby Power CPCI voltage 5 V
12	SB_5_0-VOL	02h/01h	Payload Power voltage 5 V
13	MAN_HWM_3_3-VOL	02h/01h	Standby Power CPCI voltage 3.3 V
14	MAN_IPMB_3_3-VOL	02h/01h	Standby Power LAN voltage 3.3 V
15	SB_3_3-VOL	02h/01h	Standby Power voltage 3.3 V
16	PAY_3_3-VOL	02h/01h	Payload Power PCH voltage 3.3 V
17	BAT_3_0-VOL	02h/01h	Sensor voltage 3.0 V
18	PAY_DDR4_2_5-VOL	02h/01h	Payload Power DDR voltage 2.5 V
19	PAY_130D_1_8-VO	02h/01h	Payload Power 130D voltage 1.8 V
20	PAY_DDR4_1_2-VOL	02h/01h	Payload Power DDR voltage 1.2 V
21	PAY_PCH_1_0-VOL	02h/01h	Payload Power PCH voltage 1.0 V
22	VCCST_1_0-VOL	02h/01h	Payload Power VCCST voltage 1.0 V
23	VCCIO_0_95-VOL	02h/01h	Payload Power VCCIO voltage 0.95 V
24	MAN_LAN_0_9-VOL	02h/01h	LAN Power voltage 0.9 V
25	PAY_VCORE-VOL	02h/01h	CPU Core voltage
26	PAY_VCCSA-VOL	02h/01h	Payload Power VCCSA voltage
27	PCH-TMP	01h/01h	PCH Internal Temperature
28	CPU-TMP	01h/01h	CPU Internal Temperature (PECI)
29	HWM-TMP	01h/01h	NCT7904D Temperature

3.7.2 Threshold-Based Sensors

Sensor event thresholds are classified as non-critical (NC), critical (CR), or non-recoverable (NR). This classification is possible in both directions (lower and upper). When different thresholds are reached, different actions may be executed by the shelf manager accordingly.

Table 3.4: Sensor Threshold Description

Threshold	Description
UNR	Upper non-recoverable
UCR	Upper critical
UNC	Upper non-critical
LNC	Lower non-critical
LCR	Lower critical
LNR	Lower non-recoverable

3.7.3 Voltage Sensors

The input, standby, and most payload power voltages are monitored by the BMC.

Table 3.5: Voltage Sensor List

Sensor Name	Nominal	LNR	LCR	LNC	UNC	UCR	UNR
HOT_5_0-VOL	5.00	-	4.658	-	-	5.306	-
SB_5_0-VOL	5.00	-	4.658	-	-	5.306	-
MAN_HWM_3_3-VOL	3.30	-	3.061	-	-	3.519	-
MAN_IPMB_3_3-VOL	3.30	-	3.082	-	-	3.522	-
SB_3_3-VOL	3.30	-	3.061	-	-	3.519	-
PAY_ 3_3-VOL	3.30	-	3.075	-	-	3.526	-
BAT_3_0-VOL	3.00	-	1.928	-	-	3.350	-
PAY_DDR4_2_5-VOL	2.50	-	2.331	-	-	2.671	-
PAY_130D_1_8-VOL	1.80	-	1.656	-	-	1.936	-
PAY_DDR4_1_2-VOL	1.20	-	1.088	-	-	1.304	-
PAY_PCH_1_0-VOL	1.00	-	0.904	-	-	1.096	-
VCCST_1_0-VOL	1.00	-	0.904	-	-	1.096	-
VCCIO_0_95-VOL	0.95	-	0.856	-	-	1.048	-
MAN_LAN _0_9-VOL	0.90	-	0.800	-	-	1.000	-
PAY_VCORE-VOL	0.90	-	0.208	-	-	1.568	-
PAY_VCCSA-VOL	0.90	-	0.208	-	-	1.568	

3.7.4 Temperature Sensors

Several temperature sensors are supported, either via board-populated ICs or Intel PECI readings from the CPU.

Table 3.6: Temperature Sensor List

Sensor Name	Nominal	LNR	LCR	LNC	UNC	UCR	UNR
PCH-TMP	40	-	-	-	100	104	-
CPU-TMP	50	-	-	-	100	110	-
HWM-TMP	40	-	-	-	90	100	-

3.7.5 Integrity Sensor

The integrity sensor is an OEM sensor according to the SDR (sensor data record) definitions in the IPMI specifications. It is used to observe the system during operation. If predefined conditions or actions occur, the integrity sensor throws events, generating entries in the SEL. This allows users to trace possible errors or executed actions of the firmware.

The event message contains three bytes of event data. Byte 1 is the IPMI header, which is a fixed value 0xA0. Byte 2 satisfies the logical component, while byte 3 stands for its action. The table below shows the supported event code structure generated by the integrity sensors on MIC-3399.

Table 3.7: Integrity Sensor Event Data Table

Component	Action/Subcomponent	Result	Byte 1	Byte 2	Byte3
BMC FW	Update	Successful	0xA0	0x01	0x00
	Update	Timeout	0xA0	0x01	0x04
	Update	Aborted	0xA0	0x01	0x02
	Activation	Failed	0xA0	0x01	0x21
	Manual Rollback	Initiated	0xA0	0x01	0x15
	Automatic Rollback	Initiated	0xA0	0x01	0x1D
	Rollback	Finished	0xA0	0x01	0x0E
	Rollback	Failed	0xA0	0x01	0x09
	Graceful Shutdown	Timeout	0xA0	0x01	0x74
FPGA	Update	Successful	0xA0	0x02	0x00
	Update	Timeout	0xA0	0x02	0x04
	Update	Aborted	0xA0	0x02	0x02
	Recovery	Finished	0xA0	0x02	0x0E
BIOS	Update	Successful	0xA0	0x03	0x00
	Update	Timeout	0xA0	0x03	0x04
	Update	Aborted	0xA0	0x03	0x02
	Flash 0 Boot	Failed	0xA0	0x03	0x29
	Flash 1 Boot	Failed	0xA0	0x03	0x31

3.8 OEM IPMI Commands

To provide custom, board-specific functionality, the BMC supports additional commands that are not covered by the PICMG or IPMI specifications.

Advantech management solutions support extended OEM IPMI command sets, based on the IPMI-defined OEM/Group Network Function (NetFn) codes 2Eh and 2Fh.

The first three data bytes of IPMI requests and responses under the OEM/Group Network Function explicitly identify the OEM vendor that specifies the command functionality. To be more precise, the vendor IANA Enterprise Number for the defining body occupies the first three data bytes in a request, and the first three data bytes following the completion code position in a response.

Advantech's IANA Enterprise Number used for OEM commands is 002839h. The BMC supports all Advantech IPMI OEM commands listed in the table below.

Table 3.8: OEM Command List

Command	NetFn	CMD
Set Multiplexer	2Eh	30h
Get Multiplexer	2Eh	31h
Store Configuration Settings	2Eh	40h
Read Configuration Settings	2Eh	41h
SEL Mode Configuration	2Eh	62h
Read Port 80 (BIOS POST Code)	2Eh	80h
Reload NVRAM defaults	2Eh	81h
Write MAC Address	2Eh	E1h
Read MAC Address	2Eh	E2h
Load Default Configuration	2Eh	F2h

3.8.1 Set Multiplexer Command

This command is used to set multiplexer settings. The first byte is used to select the item that should be changed; the last byte contains the new setting value.

Table 3.9: Set Multiplexer Command

	Byte	Data Field
Request Data	1:3	Advantech IANA ID (392800h)
	4	Multiplexer selection: 00h - 02h = reserved 03h = NIC 1 port 1 & 2 Other reserved.
	5	Multiplexer setting: 00h = Front 01h = Rear
Response Data	1	Completion code
	2:4	Advantech IANA ID (392800h)

3.8.2 Get Multiplexer Command

This command is used to set multiplexer settings. The first byte is used to select the item that should be read out; the answer contains the setting value.

Table 3.10: Get Multiplexer Command

	Byte	Data Field
Request Data	1:3	Advantech IANA ID (392800h)
	4	Multiplexer selection: 00h - 02h = reserved 03h = NIC 1 port 1 & 2 Other reserved
Response Data	1	Completion code
	2:4	Advantech IANA ID(392800h)
	5	Setting

3.8.3 SEL Mode Configuration Command

The storage mode (“stop on full” or “wrap/rollover”) for the SEL can be selected via the SEL mode configuration command. The already stored events will be deleted if the SEL mode is changed and the new SEL mode will start with an empty SEL list.

Table 3.11: SEL Mode Configuration Command

	Byte	Data Field
Request Data	1:3	Advantech IANA ID (392800h)
	(4)	New SEL Mode (if specified): 0 = Stop on Full Condition 1 = Wrap on Full Condition
Response Data	1	Completion code
	2:4	Advantech IANA ID (392800h)
	5	SEL Mode: 0 = Stop on Full Condition 1 = Wrap on Full Condition

3.8.4 Reload NVRAM Defaults Command

This command is used to reload the UEFI BIOS NVRAM defaults of the actual active BIOS at the next reboot. The command is only allowed when payload power is off.

Table 3.12: Reload NVRAM Defaults Command

	Byte	Data Field
Request Data	1:3	Advantech IANA ID (392800h)
Response Data	1	Completion code D5h=not supported in present state
	2:4	Advantech IANA ID (392800h)

3.8.5 Write MAC Address Command

This command can be used to change the MAC address via the BMC. The MAC address is either for the BMC's MAC (full functional impact) or for another payload device system's MAC stored in FRU data internal use area (IUA) for MAC mirroring.

Note: The non-BMC MAC addresses are written during manufacturing and are only MAC address copies for the mirroring feature. This means there is no change to the real HW MAC device.

Table 3.13: Write MAC Address Command

	Byte	Data Field
Request Data	1:3	Advantech IANA ID (392800h)
	4	MAC address number 00h = Intel(R) I210 LAN1 MAC 01h = Intel(R) I210 LAN2 MAC 02h = Intel(R) I210 LAN3 MAC 03h = Intel(R) I210 LAN4 MAC 04h = Intel(R) I210 LAN5 MAC 05h = BMC NCSI MAC
	5:10	MAC address (MSB first)
Response Data	1	Completion code
	2:4	Advantech IANA ID (392800h)

3.8.6 Store Configuration Command

This command is used to set product-specific settings. The first two bytes (Setting/ Port) are used to select the item that should be changed; the last byte contains the new setting value.

Table 3.14: Store Configuration Command

	Byte	Data Field
Request Data	1:3	Advantech IANA ID (392800h)
	4	Setting 00h - 02h = reserved 03h = Bios 04h = Lan controller 05h = Failure retries 06h = Miscellaneous 07h = RTC 08h = FPGA 09h = USB 0Ah = Clock E-keying 0Bh = PCIe 0Ch = BMC CLI 0Dh = IRQ 0Eh = Carrier Manager
	5	Setting: Bios 00h = Switch Bios Flash Setting: Lan controller 00h= LAN interface selection BI/IO Retries Reserved Setting: Miscellaneous Reserved Setting: RTC Reserved Setting: FPGA 00h = COM1 UART multiplexer 02h = BMC UART multiplexer Setting: USB Reserved Setting: Clock E-keying Reserved Setting: PCIe Reserved Setting: CLI 00h = BMC UART Baud rate Setting: IRQ Reserved Setting: Carrier Manager 01h=Graceful Shutdown timeout

Table 3.14: Store Configuration Command

Request Data	6	Setting value that is written to the selected Setting/Port Bytes Bios: Switch Bios Flash 00h = Switch Bios Flashes Lan controller: Lan interface selection 00h=Front IO interface 01h=Rear IO interface Failure Retries: Power failure retries Reserved Failure Retries: UNR Temperature retries Reserved RTC: synchronization Reserved FPGA: COM1 UART multiplexer 00h = not connected 01h = Serial-over-LAN 02h = Front panel RJ45 03h = RTM 1 FPGA: BMC UART multiplexer 00h = not connected 01h =Front panel RJ45 02h = RTM 1 CLI: BMC UART Baud rate 00h = 9600 01h = 14400 02h = 19200 03h = 38400 04h = 57600 05h = 115200 IRQ: PROC hot IRQ enabled Reserved Carrier Manager: Graceful Shutdown 00h ~ FFh = Graceful Shutdown Timeout
Response Data	1	Completion Code C7h = request data length invalid C9h = parameter out of range CBh = requested data not present D5h = not supported in present state
	2:4	Advantech IANA ID (392800h)
	5	Setting

3.8.7 Read Configuration Command

This command is used to read product-specific settings. The first two bytes (Setting/Port) are used to select the item that should be read out; the answer contains the setting value.

Table 3.15: Read Configuration Settings Command

	byte	data field
Request Data	1:3	Advantech IANA ID (392800h)
	4	Setting 00h – 02h = reserved 03h = BIOS 04h = LAN controller 05h = Failure retries 06h = Miscellaneous 07h = RTC 08h = FPGA 09h = USB 0Bh = PCIe 0Ch = BMC CLI 0Dh = IRQ 0Eh = Carrier Manager
	5	Port Setting: BIOS 00h = Active BIOS Flash Setting: LAN controller 00h = LAN interface selection front/rear IO Retries Reserved Setting: FPGA 00h = COM1 UART multiplexer 02h = BMC UART multiplexer Setting: USB Reserved Setting: Clock E-keying Reserved Setting: PCIe Reserved Setting: CLI 00h = BMC UART Baud rate Setting: IRQ Reserved Setting: Carrier Manager 01h = Graceful Shutdown Timeout
Response Data	1	Completion code C7h = request data length invalid C9h = parameter out of range CBh = requested data not present D5h = not supported in present state
	2:4	Advantech IANA ID (392800h)
	5	Setting

Table 3.15: Read Configuration Settings Command		
Response Data	6	Setting/Port Bytes Bios: Switch Bios Flash 00h = Active BIOS flash LAN controller: LAN interface selection 00h = Front IO interface 01h = Rear IO interface FPGA: COM1 UART multiplexer 00h = not connected 01h = Serial-over-LAN 02h = Front panel RJ45 03h = RTM 1 FPGA: BMC UART multiplexer 00h = not connected 01h = Front panel RJ45 02h = RTM 1 CLI: BMC UART Baud rate 00h = 9600 01h = 14400 02h = 19200 03h = 38400 04h = 57600 05h = 115200 Carrier Manager: Graceful Shutdown 00h~FFh = Graceful Shutdown Timeout

3.8.8 Read Port 80 Command

This command is used to read out the actual POST code of the UEFI BIOS.

Table 3.16: Read Port 80 Command (BIOS POST Code)		
	Byte	**Data Field**
Request Data	1:3	Advantech IANA ID (392800h)
Response Data	1	Completion code
	2:4	Advantech IANA ID (392800h)
	5	POST code

3.8.9 Read MAC Address Command

This command can be used to get the product MAC addresses.

Table 3.17: Read MAC Address Command

	Byte	Data Field
Request Data	1:3	Advantech IANA ID (392800h)
	4	MAC address number 00h = Intel(R) I210 LAN1 MAC 01h = Intel(R) I210 LAN2 MAC 02h = Intel(R) I210 LAN3 MAC 03h = Intel(R) I210 LAN4 MAC 04h = Intel(R) I210 LAN5 MAC 05h = BMC NCSI MAC
Response Data	1	Completion code D5h = not supported in present state
	2:4	Advantech IANA ID (392800h)
	5:9	MAC address

3.8.10 Reload BMC Default Configuration Command

This command reloads the product-specific settings.

Table 3.18: Reload BMC Default Configuration Command

	Byte	Data Field
Request Data	1:3	Advantech IANA ID (392800h)
Response Data	1	Completion code
	2:4	Advantech IANA ID (392800h)

3.9 HPM.1 Upgrade Support

The PICMG HPM.1 specification defines a standard way of updating (BMC) firmware components over IPMI-based interfaces. In addition to the mechanism itself, it defines a common update file format and IPMI-based commands for the update procedure. HPM.1 is the standard for firmware updates in PICMG-based environments.

Advanced features in HPM.1 address redundancy mechanisms, supporting both automatic and manual rollbacks, to support the high availability require- ments in platforms like CompactPCI.

The Advantech IPMI core G02 supports HPM.1 updates over any of its IPMI interfaces. The HPM.1 components implemented on the CPCI blade are listed in the table below.

Table 3.19: Supported HPM.1 Components

Component	Number
BMC Boot loader	0
BMC Firmware	1
FPGA	2
BIOS	3

3.9.1 Bootloader Update

The bootloader HPM.1 upgrade is written to the LPC1768 flash directly. This means there is no recovery existing for the bootloader image. It is not recommended to upgrade the bootloader in the field.

3.9.2 Firmware Upgrade

The firmware upgrade component follows the HPM.1 specification and the upgrade and activation stage can be performed while the payload is running. In case of an update, the BMC is not accessible to any service while in the activation stage.

3.9.3 FPGA Upgrade

The firmware upgrade component follows the HPM.1 specifications. The upgrade can be performed while the payload is running. For the activation stage, a payload part reboot and power off is required. The BMC is not accessible to any service while in the activation stage.

3.9.4 BIOS Upgrade

Like the FPGA component, the BIOS component requires a payload reboot or power cycle in order to perform the activation stage. The component follows the HPM.1 specifications.

3.10 Board Information

The BMC provides IPMI-defined field replaceable unit (FRU) information about the CPCI board and the connected extension modules. The MIC-3399 FRU data includes general board information such as the product name, hardware version, or serial number. A total of 2 KB of non-volatile storage space is reserved for FRU data. The boards' IPMI FRU information can be accessed via the BMC interfaces and retrieved at any time.

Table 3.20: Board Info Area-SKU1

Field Description	Board Information
Format version	0x01
Board area length	(calculated)
Language code	0x19 (English)
Manufacturer date/time	(based on manufacturing date)
Board manufacturer type/length	0xC9
Board manufacturer	Advantech
Board product name type/length	0xCB
Board product name	MIC-3399
Board serial number type/length	0xCA
Board serial number	(10 characters, written during manufacturing)
Board part number type/length	0XCB
Board part number	96923399001
FRU file ID type/length	0XEA
FRU file ID	mic-3399_sku1_fru_template_standard_0_0x.xml
Additional custom Mfg. Info fields.	(unused)
C1h (No more info fields)	0xC1
00h (unused space)	0x00 0x00 0x00 0x00 0x00
Board area checksum	(calculated)

Table 3.21: Board Info Area-SKU2	
Field Description	**Board Information**
Format version	0x01
Board area length	(calculated)
Language code	0x19 (English)
Manufacturer date/time	(based on manufacturing date)
Board manufacturer type/length	0xC9
Board manufacturer	Advantech
Board product name type/length	0xCB
Board product name	MIC-3399
Board serial number type/length	0xCA
Board serial number	(10 characters, written during manufacturing)
Board part number type/length	0xCB
Board part number	96923399011
FRU file ID type/length	0xEA
FRU file ID	mic-3399_sku2_fru_template_standard_0_0x.xml
Additional custom Mfg. Info fields	(unused)
C1h (no more info fields)	0xC1
00h (unused space)	0x00 0x00 0x00 0x00 0x00
Board area checksum	(calculated)

Table 3.22: Board Info Area-SKU3	
Field Description	**Board Information**
Format version	0x01
Board area length	(calculated)
Language code	0x19 (English)
Manufacturer date/time	(based on manufacturing date)
Board manufacturer type/length	0xC9
Board manufacturer	Advantech
Board product name type/length	0xCB
Board product name	MIC-3399
Board serial number type/length	0xCA
Board serial number	(10 characters, written during manufacturing)
Board part number type/length	0xCB
Board part number	96923399021
FRU file ID type/length	0xEA
FRU file ID	MIC-3399_sku3_fru_template_standard_0_0x.xml
Additional custom Mfg. Info fields	(unused)
C1h (no more info fields)	0xC1
00h (unused space)	0x00 0x00 0x00 0x00 0x00
Board area checksum	(calculated)

3.10.1 Product Information

Table 3.23: Product Info Area

Field Description	Product Information
Format version	0x01
Product area length	(calculated)
Language code	0x19 (English)
Product Manufacturer type/length	0xC9
Product manufacturer	Advantech
Product name type/length	0XCB
Product name	MIC-3399
Product part/model number type/length	0XCB
Product part/model number	MIC-3399
Product version type/length	0XC6
Product version	(Hardware Version)
Product serial number type/length	0xCA
Product serial number	(10 characters, written during manufacturing)
Assert Tag type/length	0xC0
Assert Tag	(unused)
FRU File ID type/length	0xEA
FRU File ID	MIC-3399_skux_fru_template_standard_0_0x.xml
Custom product info area fields	(unused)
C1h (no more info fields)	0xC1
00h (any remaining unused space)	0x00
Product area checksum	(calculated)

Appendix A

Pin Assignments

This appendix provides the pin assignments.

A.1 J1 Connector

Table A.1: J1 CompactPCI I/O							
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD(1)	5V	V(I/O)	AD(0)	ACK64#	GND
23	GND	3.3V	AD(4)	AD(3)	5V	AD(2)	GND
22	GND	AD(7)	GND	3.3V	AD(6)	AD(5)	GND
21	GND	3.3V	AD(9)	AD(8)	M66EN	C/BE(0)#	GND
20	GND	AD(12)	GND	V(I/O)	AD(11)	AD(10)	GND
19	GND	3.3V	AD(15)	AD(14)	GND	AD(13)	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE(1)#	GND
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	PCIXCAP	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
12-14	KEY AREA						
11	GND	AD(18)	AD(17)	AD(16)	GND	C/BE(2)#	GND
10	GND	AD(21)	GND	3.3V	AD(20)	AD(19)	GND
9	GND	C/BE(3)#	IDSEL	AD(23)	GND	AD(22)	GND
8	GND	AD(26)	GND	V(I/O)	AD(25)	AD(24)	GND
7	GND	AD(30)	AD(29)	AD(28)	GND	AD(27)	GND
6	GND	REQ0#	PRESENT#	3.3V	CLK0	AD(31)	GND
5	GND	NC	NC	PCI_RST#	GND	GNT0#	GND
4	GND	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	NC	TRST#	+ 12V	5V	GND
Pin	Z	A	B	C	D	E	F

Note! *NC = No connection*

 # = Active low

A.2 J2 Connector

Table A.2: J2 CompactPCI I/O

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	NC	NC	NC	GND
20	GND	CLK5	NC	NC	GND	NC	GND
19	GND	NC	GND	SMB_SDA	SMB_SCL	SMB_ALERT#	GND
18	GND	NC	NC	NC	GND	NC	GND
17	GND	NC	GND	PRST#	REQ6#	GNT6#	GND
16	GND	NC	NC	DEG#	GND	NC	GND
15	GND	NC	GND	FAL#	REQ5#	GNT5#	GND
14	GND	AD(35)	AD(34)	AD(33)	GND	AD(32)	GND
13	GND	AD(38)	GND	V(I/O)	AD(37)	AD(36)	GND
12	GND	AD(42)	AD(41)	AD(40)	GND	AD(39)	GND
11	GND	AD(45)	GND	V(I/O)	AD(44)	AD(43)	GND
10	GND	AD(49)	AD(48)	AD(47)	GND	AD(46)	GND
9	GND	AD(52)	GND	V(IO)	AD(51)	AD(50)	GND
8	GND	AD(56)	AD(55)	AD(54)	GND	AD(53)	GND
7	GND	AD(59)	GND	V(IO)	AD(58)	AD(57)	GND
6	GND	AD(63)	AD(62)	AD(61)	GND	AD(60)	GND
5	GND	C/BE(5)#	64EN#	V(I/O)	C/BE(4)#	PAR64	GND
4	GND	V(I/O)	NC	C/BE(7)#	GND	C/BE(6)#	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND
Pin	Z	A	B	C	D	E	F

Note! *NC = No connection*

 # = Active low

A.3 J3 Connector

Table A.3: J3 CompactPCI I/O (PICMG 2.16)							
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**
1	GND	PCIE_x-8_TX4-	PCIE_x-8_TX4+	VCC5	PCIE_x-8_RX4-	PCIE_x-8_RX4+	GND
2	GND	PCIE_x-8_TX0+	PCIE_x-8_RX0+	VCC5	PCIE_x-8_TX1+	PCIE_x-8_RX1+	GND
3	GND	PCIE_x-8_TX0-	PCIE_x-8_RX0-	VCC5	PCIE_x-8_TX1-	PCIE_x-8_RX1-	GND
4	GND	PCIE_x-8_TX5-	PCIE_x-8_TX5+	VCC5	PCIE_x-8_RX5-	PCIE_x-8_RX5+	GND
5	GND	PCIE_x-8_TX2+	PCIE_x-8_RX2+	PLTRST#	PCIE_x-8_TX3+	PCIE_x-8_RX3+	GND
6	GND	PCIE_x-8_TX2-	PCIE_x-8_RX2-	TAP_TMS	PCIE_x-8_TX3-	PCIE_x-8_RX3-	GND
7	GND	PCIE_x-8_TX6-	PCIE_x-8_TX6+	TAP_TCK	PCIE_x-8_RX6-	PCIE_x-8_RX6+	GND
8	GND	PCIE_CLK+	USB3_TX5+	TAP_TRST#	USB3_TX4+	USB3_RX4+	GND
9	GND	PCIE_CLK-	USB3_TX5-	TAP_TDI	USB3_TX4-	USB3_RX4-	GND
10	GND	PCIE_x-8_TX7-	PCIE_x-8_TX7+	TAP_TDO	USB3_RX5-	USB3_RX5+	GND
11	GND	GND	GND	VCC3	PCIE_x-8_RX7-	PCIE_x-8_RX7+	GND
12	GND	SATA_TX4+	SATA_RX4+	VCC3	SATA_TX5+	SATA_RX5+	GND
13	GND	SATA_TX4-	SATA_RX4-	VCC3	SATA_TX5-	SATA_RX5-	GND
14	GND	GND	GND	VCC3	GND	GND	GND
15	GND	LAN4_M-DIB1+	LAN4_M-DIB1-	GND	LAN4_M-DIB3+	LAN4_M-DIB3-	GND
16	GND	LAN4_M-DIB0+	LAN4_M-DIB0-	GND	LAN4_M-DIB2+	LAN4_M-DIB2-	GND
17	GND	LAN3_M-DIA1+	LAN3_M-DIA1-	GND	LAN3_M-DIA3+	LAN3_M-DIA3-	GND
18	GND	LAN3_M-DIA0+	LAN3_M-DIA0-	GND	LAN3_M-DIA2+	LAN3_M-DIA2-	GND
19	GND	NC	NC	SATA_LED#	NC	NC	GND

Note! *NC = No connection*

 # = Active low

**TX-input*

RX-output

A.4 J4 Connector

Table A.4: J4 CompactPCI I/O port

Pin	Z	A	B	C	D	E	F
1	GND	J4_UART_TXD	LVDS0_-CLK+	GND	DDI2_AUX+	VCC_USB4	GND
2	GND	J4_UART_RXD	LVDS0_CLK-	GND	DDI2_AUX-	USB2_D4-	GND
3	GND	J4_UART_RTS	GND	GND	NC	USB2_D4+	GND
4	GND	NC	LVDS0_D0+	GND	DDI2_TX0+	GND	GND
5	GND	GND	LVDS0_D0-	GND	DDI2_TX0-	VCC_USB5	GND
6	GND	SATA2_RX+ *	LVDS0_D1+	GND	DDI2_TX1+	USB2_D5-	GND
7	GND	SATA2_RX- *	LVDS0_D1-	GND	DDI2_TX1-	USB2_D5+	GND
8	GND	GND	LVDS0_D2+	GND	DDI2_TX2+	GND	GND
9	GND	SATA2_TX+ *	LVDS0_D2-	GND	DDI2_TX2-	DDPC_D-DC_SCL	GND
10	GND	SATA2_TX- *	LVDS0_D3+	GND	DDI2_TX3+	DDPC_D-DC_SDA	GND
11	GND	GND	LVDS0_D3-	GND	DDI2_TX3-	DDPC_HPD	GND
12-14							
15	GND	GND	LVDS1_-CLK+	GND	GND_AU-DIO	MIC_L	GND
16	GND	SATA3_RX+ *	LVDS1_CLK-	GND	NC	MIC_R	GND
17	GND	SATA3_RX- *	GND	GND	LINE1_JD	LINEIN_L	GND
18	GND	GND	LVDS1_D0+	GND	LINEOUT_L	LINEIN_R	GND
19	GND	SATA3_TX+ *	LVDS1_D0-	GND	LINEOUT_R	LOUT_L	GND
20	GND	SATA3_TX- *	LVDS1_D1+	GND	GND_AU-DIO	LOUT_R	GND
21	GND	GND	LVDS1_D1-	GND	+5V_J4_D-VIPWR	GND_AU-DIO	GND
22	GND	Erase_IN# *	LVDS1_D2+	GND	LVDS_SPC1	LCD_B-KLTEN	GND
23	GND	Erase_LED *	LVDS1_D2-	GND	LVDS_SPD1	LCD_B-KLTCTL	GND
24	GND	J4_GPIO1 *	LVDS1_D3+	GND	J4_VBAT	VDD_LVDS	GND
25	GND	J4_GPIO2 *	LVDS1_D3-	GND	J4_J2PRST#	VDD_LVDS	GND

Note! *NC = No connection*

 # = Active low

** If these signals are used, contact your local sales representative.*

A.5 J5 Connector

Table A.5: J5 CompactPCI I/O Port

Pin	Z	A	B	C	D	E	F
1	GND	LAN5_MDIA0+	LAN5_M-DIA0-	GND	LAN5_M-DIA1+	LAN5_M-DIA1-	GND
2	GND	LAN5_MDIA2+	LAN5_M-DIA2-	GND	LAN5_M-DIA3+	LAN5_M-DIA3-	GND
3	GND	LAN2_MDIB0+	LAN2_M-DIB0-	GND	LAN2_M-DIB1+	LAN2_M-DIB1-	GND
4	GND	LAN2_MDIB2+	LAN2_M-DIB2-	GND	LAN2_M-DIB3+	LAN2_M-DIB3-	GND
5	GND	NC	GND	J5_DVI-PWR	NC	NC	GND
6	GND	DDI3_AUX+	GND	DDPD_D-DC_SDA	VCC_USB7	VCC_USB6	GND
7	GND	DDI3_AUX-	GND	DDPD_D-DC_SCL	USB2_D7+	USB2_D6+	GND
8	GND	DDI3_TX0+	GND	J5_MSDAT	USB2_D7-	USB2_D6-	GND
9	GND	DDI3_TX0-	GND	J5_MSCLK	GND	GND	GND
10	GND	DDI3_TX1+	GND	J5_PS2PWR	VCC_USB8	VGA_DAT	GND
11	GND	DDI3_TX1-	GND	J5_KBDAT	USB2_D8+	VGA_CLK	GND
12	GND	DDI3_TX2+	GND	J5_KBCLK	USB2_D8-	J5_V-GAPWR	GND
13	GND	DDI3_TX2-	GND	DDP-D_HPD	GND	VGA_VS	GND
14	GND	DDI3_TX3+	GND	LAN3_LINK1000#	VCC_USB9	VGA_HS	GND
15	GND	DDI3_TX3-	GND	LAN3_LINK100#	USB2_D9+	VGA_RED	GND
16	GND	LAN5_LINK1000#	LAN2BP_LINK100#	LAN3_LINK-ACT#	USB2_D9-	VGA_GREEN	GND
17	GND	LAN5_LINK100#	LAN2BP_LINK1000#	LAN4_LINK100#	GND	VGA_BLUE	GND
18	GND	LAN5_LINK-ACT#	LAN2BP_LINK-ACT#	LAN4_LINK1000#	J5_UART_RTS	GND	GND
19	GND	R_COM1_RX#	R_COM1_CTS#	LAN4_LINK-ACT#	R_COM2_DCD#	R_COM2_TX#	GND
20	GND	R_COM1_TX	R_COM1_DSR#	RTM_PRES#	R_COM2_RTS#	R_COM2_DTR#	GND
21	GND	R_COM1_RTS#	R_COM1_DTR#	J5_UART_TXD	R_COM2_CTS#	R_COM2_RI#	GND
22	GND	R_COM1_DCD#	R_COM1_RI#	J5_UART_RXD	R_COM2_DSR#	R_COM2_RX#	GND

Note! *NC = No connection*

 # = Active low

A.6 On-Board Connector

Table A.6: SATA1 Daughter Board Connector			
1	GND	2	GND
3	SATA0_TX+	4	SATA1_TX+
5	SATA0_TX-	6	SATA1_TX-
7	GND	8	GND
9	SATA0_RX-	10	SATA1_RX-
11	SATA0_RX+	12	SATA1_RX+
13	GND	14	GND
15	GND	16	GND
17	VCC5	18	VCC3
19	VCC5	20	VCC3

Table A.7: XMC1 Connector

Pin	A	B	C	D	E	F
1	PERX_P0	PERX_N0	+3.3V	PERX_P1	PERX_N1	VPWR(+5V)
2	GND	GND	NC	GND	GND	PRST#
3	PERX_P2	PERX_N2	+3.3V	PERX_P3	PERX_N3	VPWR(+5V)
4	GND	GND	NC	GND	GND	NC
5	PERX_P4	PERX_N4	+3.3V	PERX_P5	PERX_N5	VPWR(+5V)
6	GND	GND	NC	GND	GND	+12V
7	PERX_P6	PERX_N6	+3.3V	PERX_P7	PERX_N7	VPWR(+5V)
8	GND	GND	NC	GND	GND	-12V
9	NC	NC	NC	NC	NC	VPWR(+5V)
10	GND	GND	NC	GND	GND	GA0
11	PETX_P0	PETX_N0	NC	PETX_P1	PETX_N1	VPWR(+5V)
12	GND	GND	GA1	GND	GND	MPRE-SENT#
13	PETX_P2	PETX_N2	NC	PETX_P3	PETX_N3	VPWR(+5V)
14	GND	GND	GA2	GND	GND	TBD_SDA
15	PETX_P4	PETX_N4	NC	PETX_P5	PETX_N5	VPWR(+5V)
16	GND	GND	NC	GND	GND	TBD_SCL
17	PETX_P6	PETX_N6	NC	PETX_P7	PETX_N7	NC
18	GND	GND	FPGAIO1	GND	GND	NC
19	CLK_100MHz+	CLK_100MHz-	FPGAIO2	NC(WAKE#)	NC	NC

A.7 Front I/O Connector

Table A.8: VGA1 Connector			
1	RED	9	+5V
2	GREEN	10	GND
3	BLUE	11	NC
4	NC	12	DDC_DATA
5	DET#	13	HSYNC
6	GND	14	VSYNC
7	GND	15	DDC_CLK
8	GND		

Table A.9: RJ45 LAN1/LAN2 Connector			
1	LAN_0+	5	LAN_2-
2	LAN_0-	6	LAN_1-
3	LAN_1+	7	LAN_3+
4	LAN_2+	8	LAN_3-

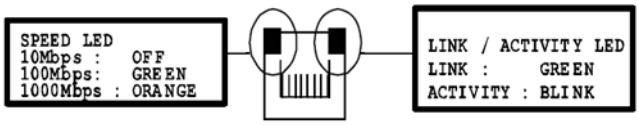


Table A.10: USB3CN1, USB3CN2, USB3CN3	
USB3CN1 / USB3CN2 / USB3CN3	
1	+5V (fused)
2	USBD1-
3	USBD1+
4	GND
5	SSRX-
6	SSRX+
7	GND
8	SSTX-
9	SSTX+

Table A.11: COM1 (RJ45) Connector			
1	DCD#	5	GND
2	SIN (RX)	6	DSR#
3	SOUT(TX)	7	RTS#
4	DTR#	8	CTS#

Table A.12: BH1 CMOS Battery			
1	BAT_VCC	2	GND

A.8 M/D, PWR, BMC, HDD, and Hot-Swappable LEDs

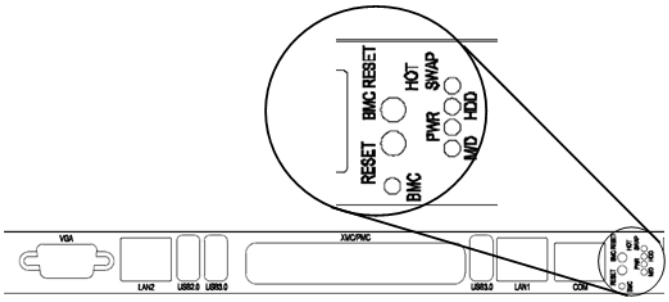


Table A.13: Front Panel LED Indicators

Name	Description
M/D (Green)	Indicates Master or Drone mode status
PWR (Green)	Indicates power status
HDD (Yellow)	Indicates HDD Read/Write
Hot Swap (Blue)	Indicates the board is ready to be hot-swapped.
BMC (Green)	Indicates BMC status

Appendix B

Programming the Watchdog Timer

This appendix describes how to program the watchdog timer.

Watchdog Timer Programming Procedure

To program the watchdog timer, users must execute a program that writes a value to the I/ O port address 943/944 (hex) to enable/disable. This output value represents the time interval. The value range is from 01 (hex) to FF (hex), and the related time interval is

1 to 255 seconds.

Data	Time Interval
01	1 sec
02	2 sec
03	3 sec
04	4 sec
...	
3F	63 sec

The countdown starts by writing a value to LPC address 0x943. The countdown can be stopped by reading 0x944. To refresh the counter, only a value has to be written again to 0x943. If the counter expires, the watchdog is reset and the state machine goes back to IDLE state.

Appendix C

FPGA Specifications

This appendix describes FPGA configuration.

C.1 Overview

Advantech's BMC solution combines an NXP LPC1768 ARM Cortex-M3-based 32-bit microcontroller and a lattice FPGA. The FPGA mainly integrates hardware interfaces that are available inside the LPC1768, like KCS.

Because MIC-3399 is available both with and without the BMC, some functions will be implemented redundantly inside the FPGA and BMC. If the BMC is populated, a simple register inside the FPGA is used to control the function from the BMC. On a MIC-3399 without BMC, the FPGA controls the function itself in the same way as before.

C.2 Features

- **Drone mode**
- **Hot-Swap Support:** Hot insertion and removal control
- **CompactPCI Backplane:** CompactPCI slot addressing
- **LPC Interface:** Provides LPC bus access
- **KCS Interface:** Standard IPMI payload interface from x86 to BMC
- **Watchdog**
- **Debug Message:** Boot time POST message

C.3 FPGA I/O Registers

The MIC-3399 FPGA communicates with the main I/O spaces. The LPC unit is used to interconnect the Intel CM236 LPC signals. The debug port unit is used to decode POST codes. The hot-swap out-of-service LED control unit is used to control the blue LED during Hot-Insert and Hot-Remove. The drone mode unit is used to disable the CPCI bridge. The other signals in the miscellaneous unit are for interfacing with the corresponding I/O interface signals.

Table C.1: LPC I/O Registers Address

LPC Address	I/O Type	Description
0x 80	W	Port 80 display
0x940	R	FPGA minor version
0x943-0x944	RW	Watchdog timer
0x945	R	FPGA major version
0x946	R	BIOS flash control
0x947	R	Geographical address (GA)
0x948	R	MISC STS
0x94C	R	FPGA ID
0x94D	R	BMC MUX
0x94E	R	COM1 MUX
0x94F	RW	Scratch register
0xCA2 ~ 0xCA3	RW	KCS interface

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Please verify specifications before quoting. This guide is intended for reference purposes only.